e-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication

S. Bonacini[1], K. Kloukinas[1], and P. Moreira[1]
[1]CERN, European Organization for Nuclear Research, Geneva, Switzerland

Abstract

The e-link, an electrical interface suitable for transmission of data over PCBs or electrical cables, within a distance of up to 2 m, at data rates up to 320 Mbit/s, is presented. The e-link is targeted for the connection between the GigaBit Transceiver (GBTX) chip and the Front-End (FE) integrated circuits. A commercial component complying with the Scalable Low-Voltage Signaling (SLVS) electrical standard was tested and demonstrated a performance level compatible with our application. Test results are presented. An SLVS transmitter/receiver IP block was designed in 130 nm CMOS technology. A test chip was submitted for fabrication.

Introduction

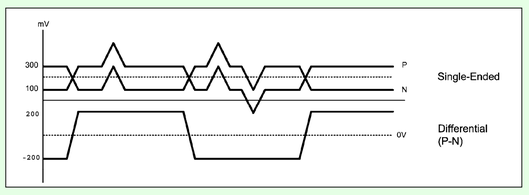
With the future upgrade of the LHC and its associated experiments the number of detector channels will increase and it is thus necessary to envisage new low-power interconnections schemes for the on detector Application-Specific Integrated Circuits (ASICs). These schemes will allow to reduce the material budget due to cabling and cooling. For this purpose, numerous slow data links could be aggregated into fewer faster and more efficient links.

The GBT project was started to design the future optical data link for the experiments, which brings together the functions of data readout, trigger and control. The GBT will be connected to up to 32 FE ASICs, requiring each one a dedicated electrical link, in a star-point topology. These links target short distance transmission (typically up to 2 meters on PCB, and up to 4 meters on cable) and shall not inject noise in the FE detectors and ASICs. In addition, the links should be designed to minimize crosstalk, sensitivity to common-mode and power supply noise.

For these reasons, the study of a low-power low-voltage-swing electrical link was carried out. Among the several link protocols examined, the Scalable Low-Voltage Signaling (SLVS) industry standard was chosen and tested.

The SLVS standard

The SLVS standard is defined in [1] and describes a differential current-steering electrical protocol with a 200 mV voltage swing on a 100 Ω load and with a common mode of 200 mV. The differential voltage is therefore 400 mV.

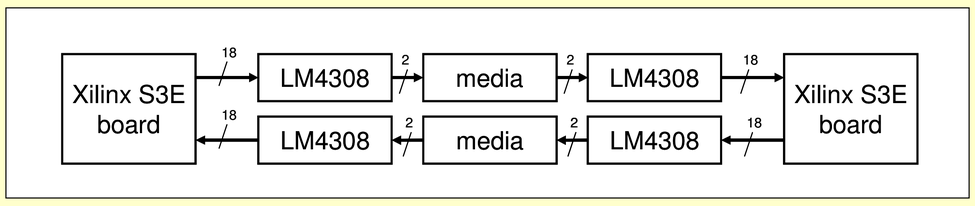


A few commercial parts which comply to this standard are available, mainly from National Semiconductors. Their target applications are in mobile/portable devices for short (< 30 cm) communication links over PCB traces and flat cable.

Bit Error Rate Testing

A commercial part which uses the SLVS standard was tested with several media types and lengths (5 m Ethernet cable, 30 cm kapton, 2 m PCB and others) at two different speeds (320 Mbps and 480 Mbps). The test aimed to demonstrate the capability of the electrical protocol to work with longer distances and different media than the part's typical application. The part we used is the LM4308 from National Semiconductors.

The test setup is composed of
(a) Two Xilinx Spartan-3E evaluation boards,
(b) Two custom PCBs holding each two LM4308 components,
(c) Two link media,
arranged like in the figure (clock signals are not shown).



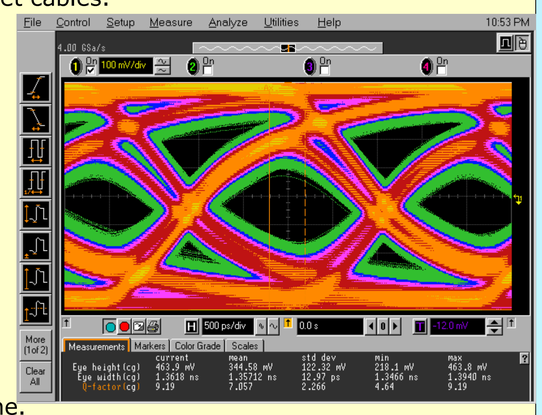
The LM4308 chip is an SLVS serdes, which can be hardwire-configured to be either a serializer or a deserializer. In the test, two LM4308 chips are serializers while the other two are deserializers.

Each Xilinx Spartan-3E chips generates a pseudo-random sequence, which is fed to a serializer, and checks the sequence coming from a deserializer. The link media are connected to the serdes boards through Samtec QTE/QSE connectors.

Several media were tested. A few special PCB-type media were fabricated for this purpose: a 1 m microstrip, a 2 m microstrip and a 2 m stripline; these lines follow a serpentine path to minimize area. An Ethernet plug adapter was also fabricated in order to test Ethernet cables.

The test results are described in the following table:

	320 Mbps	480 Mbps
1m microstrip	< 1.E-13	< 1.E-13
2m microstrip	< 1.E-13	< 1.E-13
2m stripline	< 1.E-13	< 1.E-13
24 cm Kapton	< 1.E-13	< 1.E-13
5m ethernet cable	1.E-13	2.E-11



The eye-diagram on the right has been obtained at 480 Mbps at the load of a 2-m microstrip PCB line.

It should be noted that the LM4308 uses a forwarded-clock technique, therefore errors might as well come from the clock line.

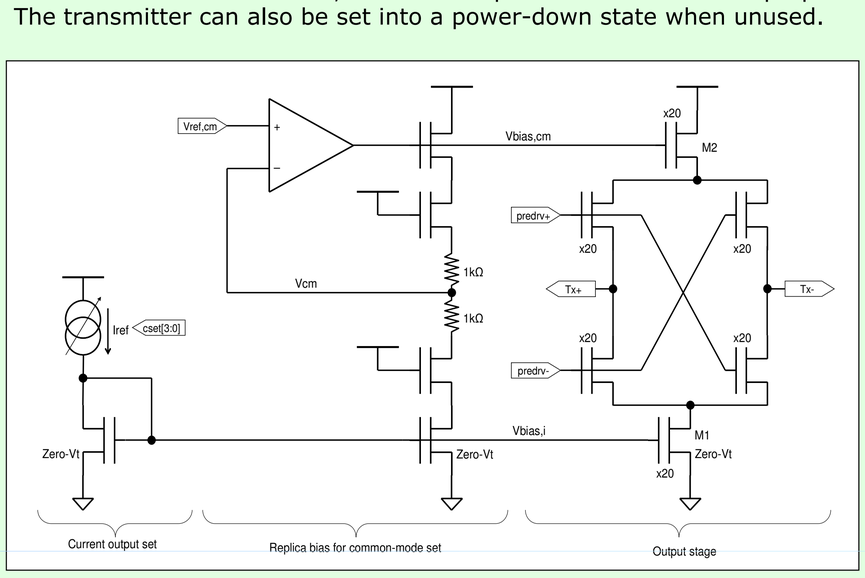
The results of the test demonstrate that the SLVS electrical standard is a potential candidate for the implementation of the chip-to-chip interconnections for FE ASICs.

SLVS transmitter and receiver IP blocks design

A transmitter and receiver IP blocks for integration in the FE ASICs, complying with the SLVS protocol, were designed in a 130 nm technology. The e-link can operate at any speed up to 320 Mbps. The transmitter and receiver blocks are designed to work in the harsh environment of the experiments characterized by high level of radiation (up to hundreds of Mrads) and intense magnetic field (up to 4 T). Though these IP blocks are targeted for the implementation of the GBTX-FE connection, they are also suitable for general chip-to-chip communication within the LHC experiments.

The transmitter and receiver circuits are designed to be powered in the range from 1.0 to 1.5 V.

Transmitter: In order to minimize the power consumption, the current output is adjustable from 2 mA down to 0.5 mA, with a 60% power reduction and a proportional lowering of crosstalk. The transmitter can also be set into a power-down state when unused.



The transmitter is implemented by a N-over-N driver which steers the current given by the current source M1. The current is set by a 4-bit digital switch (not in the figure).

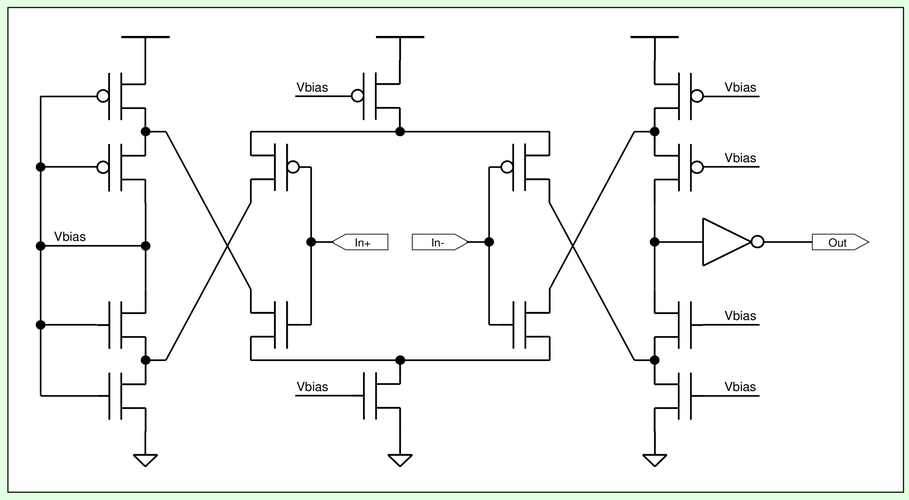
The common-mode is kept at $V_{ref,cm}$ = 200 mV by the replica bias of the source-follower M2.

In power-down mode, all the biasing circuits are switched off and the pre-driver stops toggling the final stage.

The transmitter consumes 3 mW at 320 Mbps, 1.2 V power supply and with 2 mA output.

Receiver: The receiver is implemented by a rail-to-rail differential amplifier such that it guarantees a wide common-mode voltage range. The receiver can be set into a power-down state when unused.

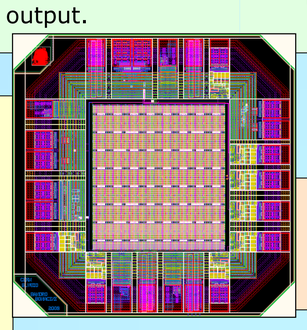
The first stage amplifier, similar to [2], is a combination of two basic complementary amplifiers, which together can cover fully the input range from negative to positive supply. Moreover, the amplifier is self-biased through negative feedback.



In power-down mode the biasing is switched off. This prevents toggling on the output.
The receiver consumes 210 µW at 320 Mbps, 1.2V supply and with a 64 fF output load.

Test chip

A test chip containing the SLVS receiver and the SLVS transmitter was designed and submitted for fabrication. The test chip works as an LVDS-to-SLVS translator and vice-versa. A few CMOS input pins are present to control the transmitter current output setting and the receiver shutdown. A loopback control pin is also provided for testing. Testing will be performed on the chip to evaluate the bit error rate in the same fashion as the commercial part.



[1] JESD8-13,"Scalable Low-Voltage Signaling for 400 mV (SLVS-400)", JEDEC.
[2] M. Bazes, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, Feb. 1991.