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e-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication

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the e-link, an electrical interface suitable for transmission of data over PCBs or electrical cables, within a distance of a few meters, at data rates up to 320 Mbit/s, is presented. The e-link is targeted for the connection between the GigaBit Transceiver (GBTX) chip and the Front-End (FE) integrated circuits. A commercial component complying with the Scalable Low-Voltage Signaling (SLVS) electrical standard was tested and demonstrated a performance level compatible with our application. Test results are presented. A SLVS transmitter/receiver IP block was designed in 130 nm CMOS technology. A test chip was submitted for fabrication.

Summary

With the future upgrade of the LHC and its associated experiments the number of detector channels will increase and it is thus necessary to envisage new low-power interconnections schemes among the on detector ASICs which will allow to reduce the material budget due to cabling and cooling. For this purpose, numerous slow data links could be aggregated into fewer faster and more efficient links.

The GBT project was started to design the future optical data link for the experiments, which brings together the functions of data readout, trigger and control. The GBT will be connected to a number of up to 32 FE Application-Specific Integrated Circuits (ASICs), requiring each one a dedicated electrical link, in a star-point topology. These links target short distance transmission (typically up to 2 meters on PCB, and up to 4 meters on cable) and shall not inject noise in the FE detectors and ASICs. In addition, the links should be designed to minimize crosstalk, sensitivity to common-mode and power supply noise.

For these reasons, the study of a low-power low-voltage-swing electrical link was carried out. Among the several link examined, the Scalable Low-Voltage Signaling (SLVS) industry standard was chosen and tested. The standard describes a differential current-steering electrical protocol with a 200 mV voltage swing on a 100 Ohm load and a common mode of 200 mV. The differential voltage is therefore 400 mV.

A commercial part which uses the SLVS standard was tested with several media types and lengths (5 m Ethernet cable, 30 cm kapton, 2 m PCB and others) and demonstrated bit error rates of less than 10-13 at 480 Mbps on PCB and kapton links, while less than 10-10 on Ethernet STP cable. The article will present the results of the tests.

A transmitter/receiver IP block for integration in the FE ASICs, complying with the SLVS protocol, was designed. In order to minimize the power consumption, the current output of the transmitter is adjustable from 0.5 mA to 2 mA, with a 60% power reduction and thus proportional lowering of crosstalk. Both transmitter and receiver can also be set into a power-down state when unused. The receiver is implemented by a rail-to-rail differential amplifier such that it guarantees a wide common-mode voltage range. The e-link can operate at any speed up to 320 Mbps. The transmitter/receiver block is designed to work in the harsh environment of the experiments characterized by high level of radiation (up to hundreds of Mrd) and intense magnetic field (up to 4 T). The article will presents in detail the design of the transceiver circuit.

Though this IP block is targeted for the implementation of the GBTX-FE connection, it is also suitable for general chip-to-chip communication within the LHC experiments.

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