A Zero Suppression Micro-Circuit for Binary Readout CMOS Monolithic Sensors

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Abstract

The EUDET-JRA1 beam telescope and the STAR vertex detector upgrade will be equipped with CMOS pixel sensors allowing to provide high density tracking adapted to intense particle beams. The EUDET sensor Mimosa26, is designed and fabricated in a CMOS-0.35µm Opto process. Its architecture is based on a matrix of 1152x576 pixels, 1152 column-level Analogue-to-Digital Conversion (ADC) by discriminators and a zero suppression circuitry. This paper focused on the data sparsification architecture, allowing a data compression factor between from 10 and 1000, depending on the hit density per frame. It can be extended to the final sensor for the STAR upgrade.

I. INTRODUCTION

CMOS Monolithic Active Pixel Sensors (MAPS) are characterized by their detection efficiency close to 100 % , high granularity (~µm), fast read-out frequency (~k frame/s), low material budget (~30 µm Si) and radiation tolerance (~1 Mrad, ~10^{13} n_{eq}/cm^2). They are foreseen to equip new generation of vertex detectors in subatomic physics experiments [1]. Their first application coincides with the upgrade of the Heavy Flavor Tracker (HFT) in the STAR (Solenoidal Tracker at RHIC) experiment [2]. They will also equip the beam telescope of the European project EUDET [3]. The aim of the EUDET-JRA1 project is to support the infrastructure for doing detector R&D (Detector R&D towards the Internal Linear Collider). One of activities is to provide a CMOS pixel beam telescope to be operated initially at the DESYII 6 GeV electron test beam facility, near Hamburg in Germany. The high precision beam telescope will be built with up to six measurement planes equipped with CMOS Monolithic Active Pixel Sensors (MAPS). Both of these two applications need sensors with digital output and with integrated zero suppression circuit in order to increase the read-out frequency per frame with the aim to reduce the frame occupancy. The zero suppression circuit integrated in a CMOS pixel sensor is located at the bottom of a matrix and after an analogue to digital conversion circuit. Mimosa26 [4] designed for the EUDET telescope, implements such architecture. It consists of a pixel array of 576 rows and 1152 columns with a pixel pitch of 18.4 µm. Each pixel includes amplification and a Correlated Double Sampling (CDS) and each column of pixels ends with a discriminator performing the analogue to digital conversion. The data from 1152 discriminators are processed by the zero suppression circuit. Before its integration into a final sensor, the concept of the zero suppression logic has been validated. SUZE-01, a reduced scale, fully digital circuit, able to treat and format 128 emulated discriminator outputs, has been successfully fabricated and tested in 2007. The test shows that the algorithm of hits pixel selection is fully operational. This concept is now implemented into the Mimosa26 chip. The first part of this paper describes the overview of the readout sensor architecture. The second part presents the zero suppression algorithm for MAPS architecture witch is structured in 3 steps. The last section is dedicated to the test methodology for digital output sensor.

II. OVERVIEW OF THE SENSOR ARCHITECTURE

A. Hit recognition and encoding format

The sensor is read out in a rolling shutter mode, the rows being selected sequentially by activating a multiplexer every 16 clock cycles. Figure 1 shows an example of digital matrix frame with some hits. Their coding is performed in terms of "states", each representing such a group of successive pixels giving a signal above discriminator threshold in a row. The "state" format includes the column address of the first hit pixel, followed by 2 bits encoding the number of contiguous pixels in the group delivering a signal above threshold. The row address is represented by an 11 bit number and is common to all "states" in a row. Up to M "states" by row can be processed. This limit was derived from a statistical study based on the highest occupancy expected in the pixel array.

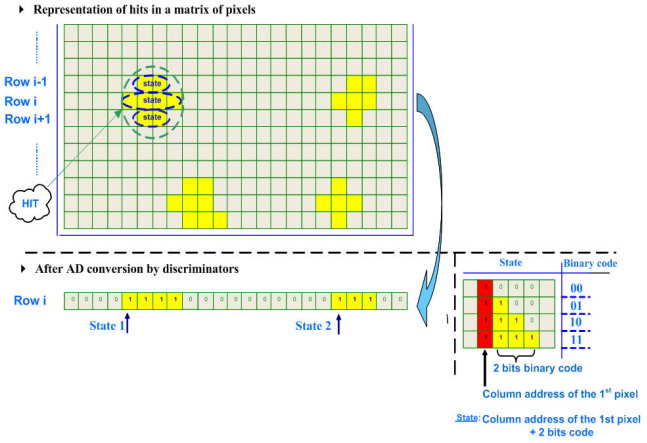

Figure 1: Schematic view illustrating the encoding of the pixels delivering a signal above discriminator threshold

B. Principle of hit finding algorithm

The zero suppression logic [5] is based on sparse-scan read-out [6] in order to optimize the data bandwidth. A fast priority scan path between the first and last discriminator outputs is implemented to minimize the delay within the critical data path. The 1152 column terminations are distributed over 18 banks (see Figure 2), each bank being connected to 64 columns. The digital architecture allowing to find '1's in a row of discriminated outputs is based on "Sparse Data Scan" algorithm.

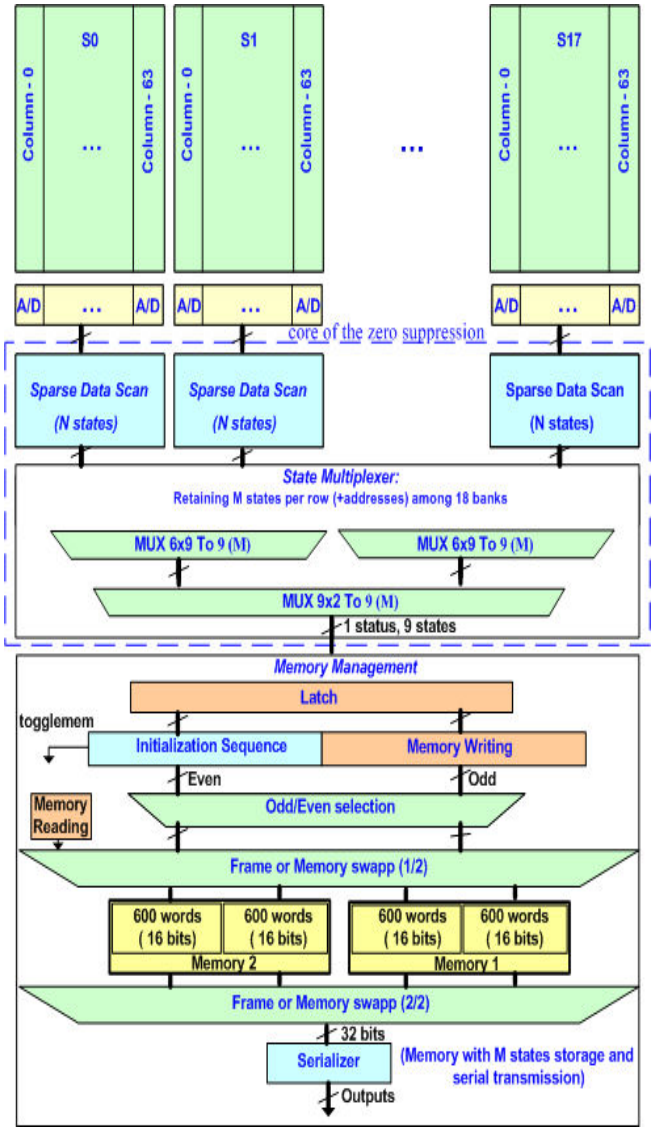

Figure 2: Block diagram of the sensor read-out architecture

III. Zero Suppression for MAPS Architecture

A. Fast readout architecture of MAPS

The digital part sequentially controls each line for the whole frame composed of 576 lines of 1152 columns. The main sequencer gives the address of lines and all synchronizations and controls signals (see Figure 3) and works at 80 MHz.

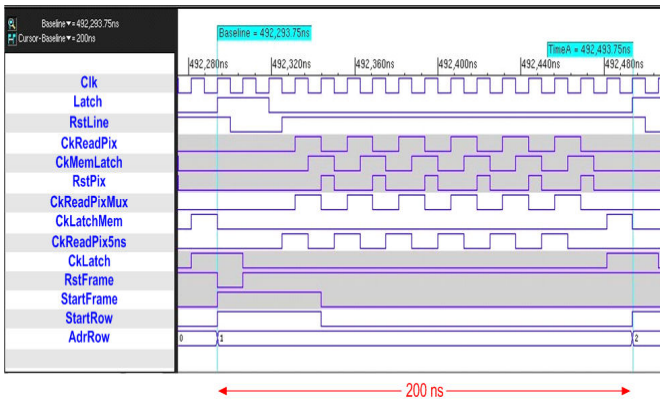

Figure 3: Timing diagram for suze control signals

A JTAG controller programs the configuration information. The row of matrix is read during 200 ns and the read out frame frequency is about 10 KHz.

B. Readout Chain

Zero suppression is based on row by row sparse data readout and organized in pipeline mode in three steps.

1) Sparse data scan

Figure 4 shows the different steps of the sparse data scan for one bank.

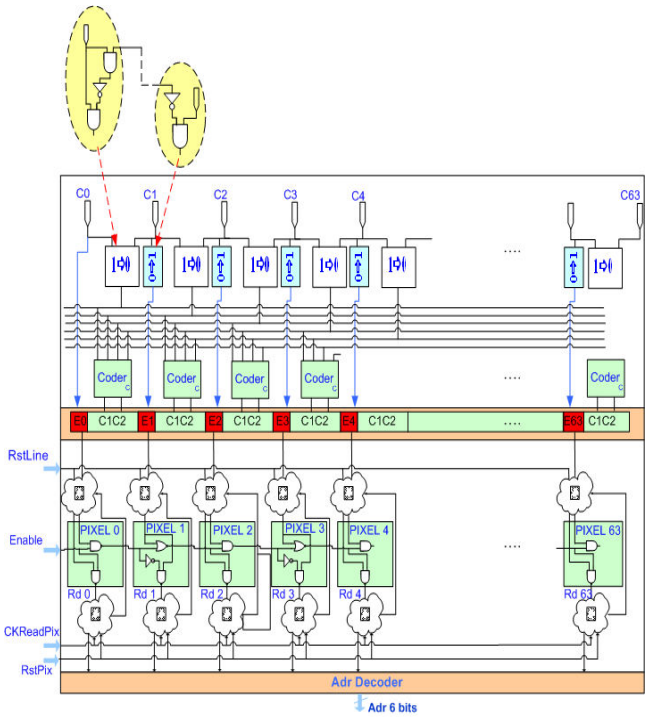

Figure 4: Schematic view of sparse data scan for one bank

The algorithm proceeds through four consecutive steps, summarized below:

- In the first step, the data inputs for the process are extracted from 64 discriminators;
- The second step consists in encoding groups of hit pixels. This logic provides Enable bits and Code bits for each column composing a bank. The Enable bit is set to 1 for the

first hit pixel in a group. The number of Enable bits set to 1 characterizes the state;

- The third step selects the "states"; each "state" is selected successively by a sparse data scan. It uses a chain of alternated NAND and NOR gates for the priority management during the sparse-scan. The generation of "states" requires several instructions. The number of "states" (N) in a bank is related to M "states" in a row. The algorithm manages up to N=6 instructions or "states" in a bank;
- At each instruction, the column address of the "state" is decoded. The last digital step stores the N "states" and generates "status" information indicating the number of "states" per bank. Each bank has its own address encoded in 5 bits.

2) State Multiplexer

The state Multiplexer reads out the outcomes of the first step in 18 banks and keeps up to M=9 "states". For a row, each bank provides a maximum of N "states". Another logical unit, based on multiplexers, allows selecting a maximum of M "states" among 18xN (bank) "states". Thus, maximum M "states" will be stored in a memory. In case of more than M "states" are identified, an overflow bit is set to 1. The format of the row "states" includes the row address, the status register (number of states in the entire row), the "state" column addresses and the overflow bit.

This block is constituted of 3 sub-blocks:

- 2 identical modules Mux6x9To9, extracting each 9 "states" and 1 status for an half row
- 1 module Mux2x9To9, retaining 9 "states" and a status from these 2 modules

After the active state of RstLine, the process starts by scanning the result of 18 banks starting from column 0 to 1151. The enable signal for the CkReadPixMux clock, allows doubling the clock period for the logic, which is most critical part in the design. The algorithm of module Mux6x9To9 (see Figure 5) read 9 hits "states" at maximum in 3 steps. At each rising edge of enabled CkReadPixMux (T=CK1, CK2, CK3), 3 hits "states" can be latched at maximum and each step proceeds through 3 consecutive stages, described below:

- *Cursor 1* is located on:
  - First hit "state"
- *Cursor 2* is located either:
  - at the fourth hit "state" if it belongs to the same bank pointed by Cursor 1
  - or at the second or third hit "state" if the "state" is in a different bank used by the Cursor 1
  - or at the Cursor 1 location if there is no hit anymore
- *Cursor 3* is located either:
  - at the third hit "state" after the Cursor 2 location if this "state" belongs to the same bank pointed by Cursor2
  - or at the first hit "state" if the "state" is a different bank pointed by the Cursor 2
  - or at the Cursor 2 location if there is no hit anymore

At the second CK2 and third CK3 rising edge: Cursor 1 points on the previous location of the Cursor 2 or 3, according to the hit "states" configuration. Cursor 2 and Cursor 3 locations are updated following the same processing realized during the phase of CK1.

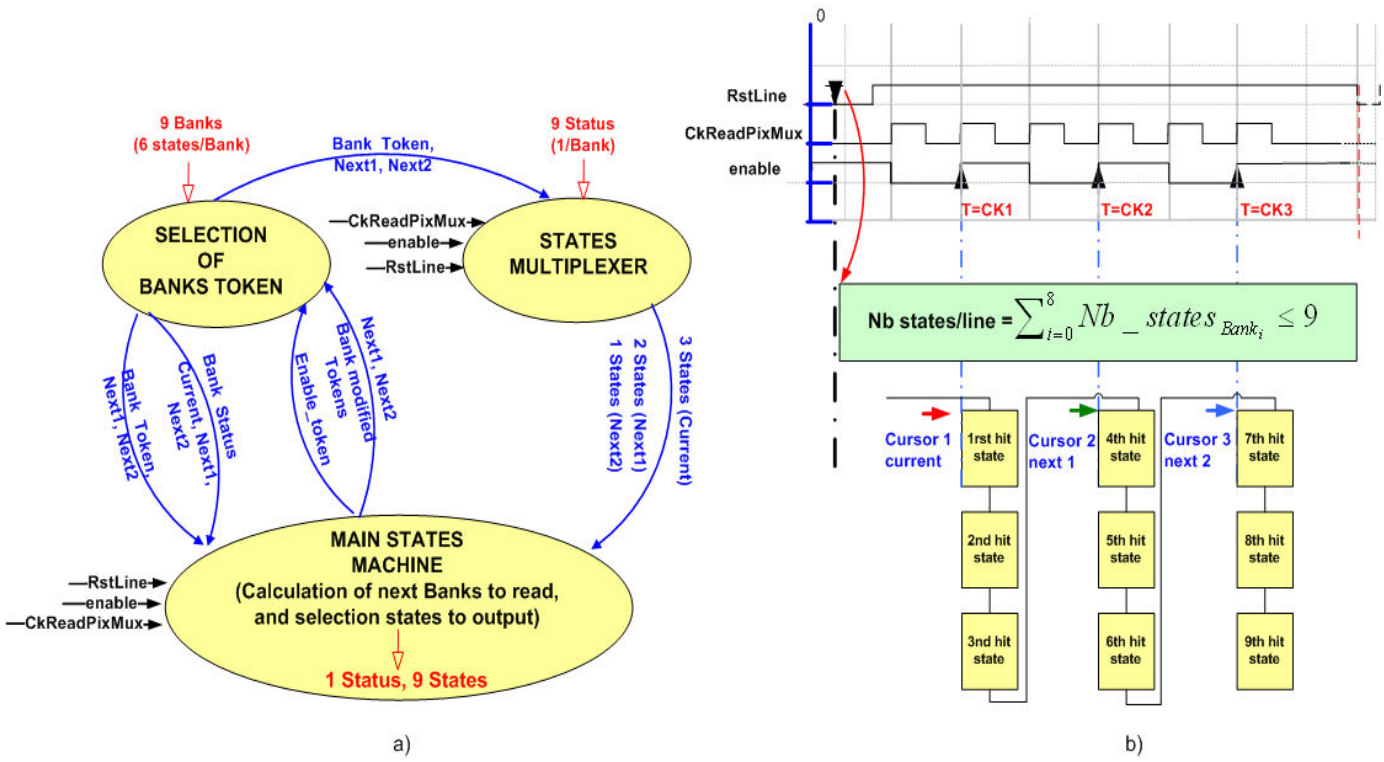

Figure 5: View of Mux6x9To9 algorithm

3) Memory management

This step corresponds to storing the outcomes of *state multiplexer* step to a memory.

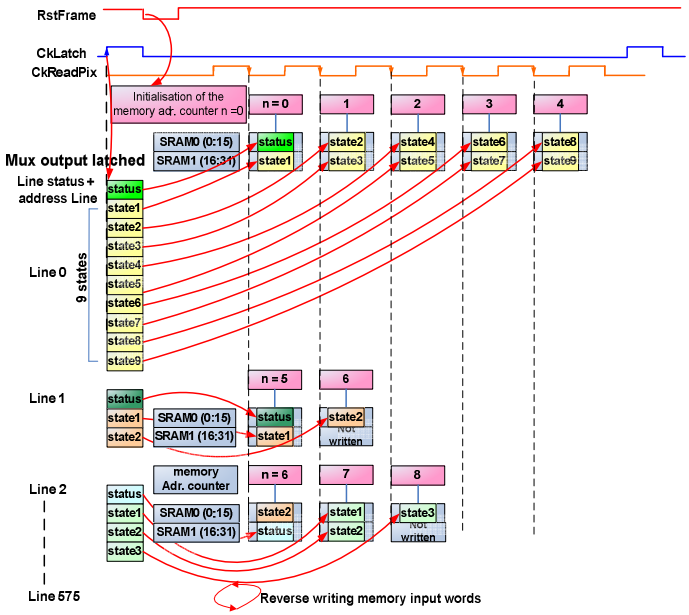

Figure 6: Memory manager of hits "states"

Memory is composed of 2 IP's buffers to ensure the continuous read-out (4 SRAM's: 600 x 16 bits each, see Figure 2):

- During the current frame, the writing mode uses 2 SRAM's and the reading mode works with 2 others SRAM's.
- The writing process is realized by the writing of word of 2x16 bits. In order to reduce the useful memory space (see Figure 6), if the last word of 16 bits is not written (in case of even number of hit states in the current row), next row processing status is written in that location.
- At the end of the frame, a state machine memorizes the number of written words given by the address writing counter.

During the next frame, the 2 operations (reading/ writing) are swapped, and this process is repeated at each frame.

The format of the row "states" is composed of Status/line and State words. *States/Line* contains the address of the line which is hit, the number of "state" for this line (i.e. a number between one and nine), and an overflow flag. "State" contains the address of the first hit pixel and the number of successive hit pixels as shown on the Figure 7. Two low voltage differential signalling (LVDS) data lines (DO0 and DO1) are used for the data transmission (frequency is 80 MHz).

The Figure 7 describes the format of data send by Mimosa26. The different part of the data frame is the *Header*, *Frame counter*, *Data Length*, *States/Line*, *State*, and *Trailer*. The 2 words elements (i.e. *Header*, *Frame counter*, *Data Length* and *Trailer)* are divided into two parts. For instance, the header includes Header0 (corresponds to the 16 bits LSB) and header1 (corresponds to the 16 bits MSB). The *Header*, the *Trailer* could be used together to detect loss of synchronization.

DataLength is the number of words (16 bits) of the useful data. The data periodically sent at the beginning of each new frame, and the number of bits sent between two headers is variable and depends on the numbers of the words recorded during the last frame. Both data lines have the same number of bits. Consequently *Datalength0* and *Datalength1* are the same. The useful data are represented by the daisy chain of *States/Line* and *States*. The maximum number of the data generated by the suppression of zero is 570 x 16 bits for each output. After this overflow, the data frame will be truncated. Besides, the data rate per output reaches around 10 Mbytes/s.

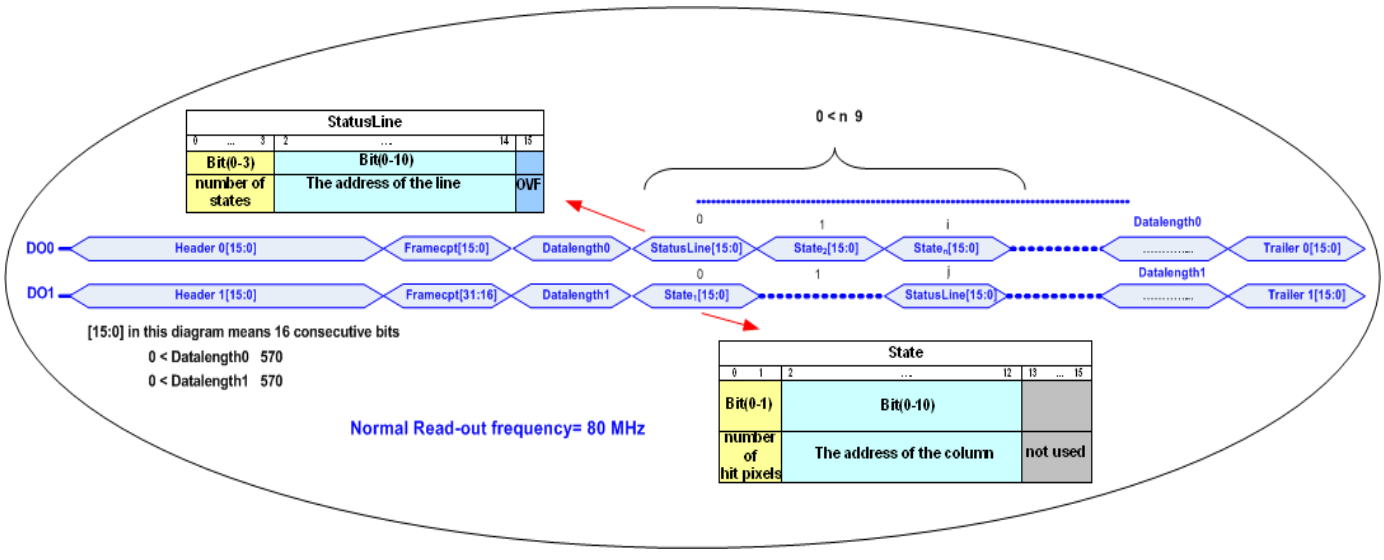

Figure 7: Format of the Mimosa 26 output data : 80 MHz dual channel

IV. Digital Output Sensor

A. Chip architecture

The Figure 8 shows Mimosa 26 layout: the 1st sensor integrating the zero suppression feature, fabricated the beginning of 2009. The zero suppression logic, located at the bottom of 1152 discriminators, occupies an area of 21.5 x 0.62 mm^2. It is based on SUZE-01 prototype. The propagation delay for such dimensions becomes preponderant at 80 MHz and involves some difficulties for layout routing (digital part). The layout includes 70K standard cells. A JTAG controller embedded allows the communication between the core of the system and an external test structure. The fabrication process is the AMS C35B4C3 CMOS 0.35 µm technology, already used in MIMOSA pixel sensors.

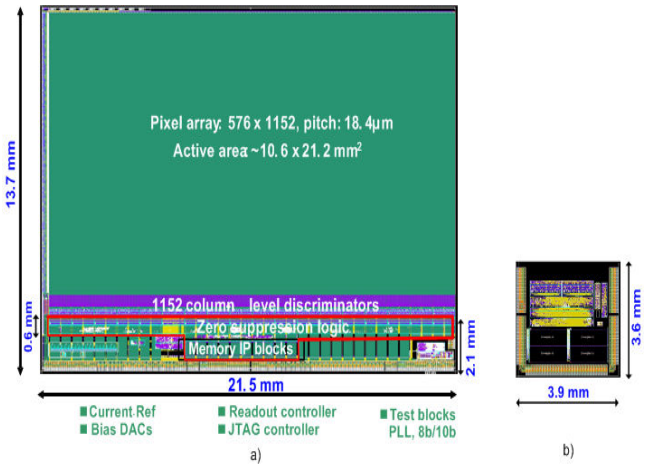

Figure 8: a) Mimosa 26 layout: 1st sensor with Integrated Zero Suppression b) SUZE-01 prototype: Zero Suppression circuit

B. Test Sensor with Integrated zero suppression

The tests of the chip require specific board. The dedicated communication through the JTAG protocol is initiated by a user interface written in C (Windows environment). This user interface configures registers for the initialisation sequence. We introduce all parameters for the synchronization of the acquired frame, and two lines pattern. The ASIC includes an embedded structure of test. This structure generates a matrix constituted of 278 times the two lines pattern. Each part of the architecture can be tested separately or entirely. The Mimosa26 test board, at the end of chip, is connected to the platform NXI (National Instruments) acquiring the data stream at 160 Mbits/s (see Figure 9). For the tests performance, in automatic way, the data patterns are selected from a source text file and sent through the chip via the JTAG interface. All the features of the architecture were tested successfully: encoding of the hit (location and geometry) and the limits of the data compression system. We can note also additional tests for reliability and robustness:

- Reliability test: 3 patterns tested 7 millions times without error.
- Robustness test: 199 frames x 10 000 random patterns test at 80 MHz without error.

The full chain test including the pixel matrix, discriminators, and the zero suppression logic, can be found in the reference [7].

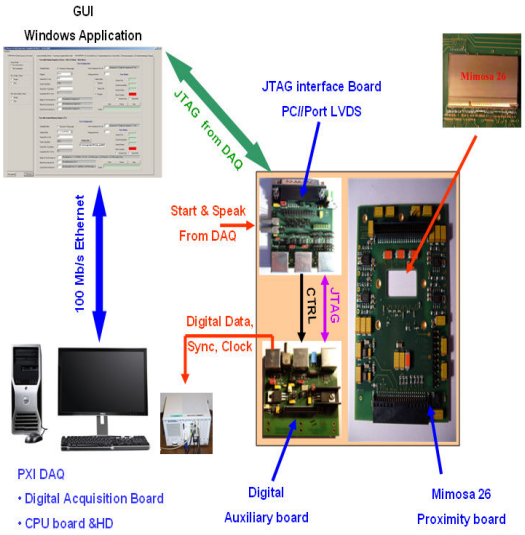

Figure 9: Schematic view of the test set-up of Mimosa 26

V. Conclusions

In this paper, we have designed a fast read-out architecture witch integrates zero suppression circuit, based on sparse data scan. The readout speed is ~10 kframe/s. The Mimosa26 readout chain was validated by functionality tests in laboratory. Consequently, the data flow reduction will allow running the EUDET telescope on high intensity particle beams. The sensor for the HFT upgrade in STAR will be based on Mimosa26 architecture and is planned to be manufactured in 2010.

VI. References

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