The GBTIA, a 5 Gbit/s Radiation-Hard Optical Receiver for the SLHC Upgrades

M. Menouni [a], P. Gui [b], P. Moreira [c]

[a] CPPM, Université de la méditerranée, CNRS/IN2P3, Marseille, France
[b] SMU, Southern Methodist University, Dallas, Texas, USA
[c] CERN, European Organization for Nuclear Research, Geneva, Switzerland

menouni@cppm.in2p3.fr

Abstract

The GigaBit Transceiver (GBT) is a high-speed optical transmission system currently under development for HEP applications. This system will implement bi-directional optical links to be used in the radiation environment of the Super LHC. The GigaBit Transimpedance Amplifier (GBTIA) is the front-end optical receiver of the GBT chip set.

This paper presents the GBTIA, a 5 Gbit/s, fully differential, and highly sensitive optical receiver designed and implemented in a commercial 0.13 µm CMOS process. When connected to a PIN-diode, the GBTIA displays a sensitivity better than −19 dBm for a BER of 10^{-12}. The differential output across an external 50 Ω load remains constant at 400 mV_{pp} even for signals near the sensitivity limit. The chip achieves an overall transimpedance gain of 20 kΩ with a measured bandwidth of 4 GHz. The total power consumption of the chip is less than 120 mW and the chip die size is 0.75 mm x 1.25 mm. Irradiation testing of the chip shows no performance degradation after a dose rate of 200 Mrad.

I. Introduction

The GBTIA chip consists of a low-noise, high-bandwidth transimpedance amplifier (TIA) and a high performance limiting amplifier (LA) followed by a 50 Ω output stage to achieve high gain and high bandwidth. The photodiode biasing circuit is integrated in the same chip. Figure 1 shows the block diagram of the GBTIA receiver.

The TIA adopts a differential cascode structure (Figure 1) with series inductive peaking to achieve high transimpedance gain, high bandwidth, and low input referred noise. The Photo Detector (PD) current is AC coupled to the TIA using on-chip capacitors. The capacitive coupling rejects the DC component of the PD signal and allows for a fully differential structure with high power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) to be used.

To cope with a potentially high leakage current in the PD induced by radiation, a novel PD biasing circuit is designed in the TIA to ensure the proper biasing of the PD for a leakage current ranging from 1 pA to 1 mA.

The LA is composed a cascade of four limiting amplifier stages followed by a 50 Ω output stage to achieve high gain and high bandwidth. Each limiting stage employs a modified Cherry-Hooper structure with resistive loading and active inductive peaking to enhance the bandwidth. The four limiting stages are sized with increasing currents and transistor dimensions to be capable of delivering 8 mA to the output load while maintaining a high bandwidth. The GBTIA chip has been tested with a high-frequency PD at room temperature.

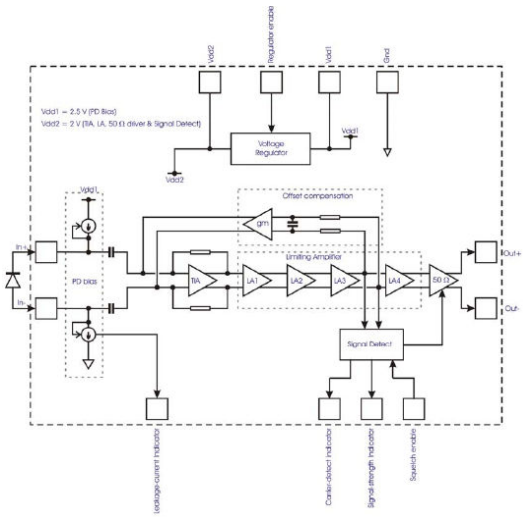

Figure 1 : The Block Diagram of the GBTIA Receiver

In section II, the architecture of the transimpedance amplifier is described and analyzed. Section III presents the design of the limiting amplifier. In section IV, the effect of the leakage current is analyzed and finally section V is dedicated to the presentation of the experimental results.

II. Transimpedance Amplifier Design

Figure 2 shows the TIA schematic diagram. As mentioned before, a differential configuration was adopted for its high PSRR and CMMR (although at a small sensitivity penalty). This ensures low cross-talk between the first stage and subsequent stages allowing for integrating the three functions: pre-amplifier, limiting amplifiers and 50 Ω driver in a single chip.

A high current level is needed for the input transistor to achieve high cut-off frequency and low noise. Consequently the input transistor size becomes large and

the parasitic capacitance reaches a high value. The cascode structure eliminates the effect of Miller capacitance and enhances the bandwidth.

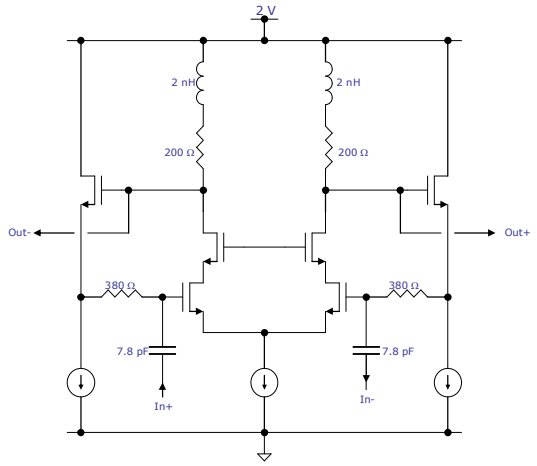

Figure 2 : Schematic diagram of the transimpedance amplifier

The bandwidth of the transimpedance amplifier is determined by the total capacitance at the input node, the total input resistance of the preamplifier and the open loop gain of the amplifier.

The capacitance of the input node is defined by the photodiode and the bond-pad capacitance. It is difficult to increase the open loop gain of the amplifier to a value higher than 10 because of the relatively low transconductance g_m of the MOS transistors. The input resistance can be reduced by decreasing the feedback resistor R_F, but additional thermal noise is induced due to the lower value of the feedback resistance and therefore the sensitivity of preamplifier is degraded. In order to meet the low noise and wide bandwidth characteristics simultaneously, the shunt peaking technique was used in the TIA stage.

Figure 3 shows that the bandwidth can be significantly improved by using the shunt peaking technique. However, this comes at the cost of significant gain peaking which introduces Inter Symbol Interference (ISI). For this reason, the inductance value is sized to work at optimum group delay where the bandwidth is extended by less than 40 %.

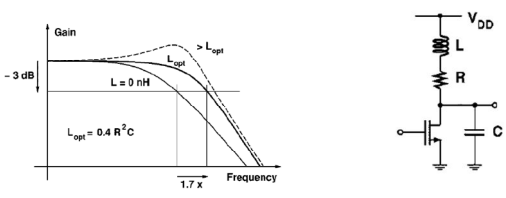

Figure 3 : Bandwidth extension with shunt peaking

III. Limiting Amplifier Design

A. *Design consideration and the overall architecture of the limiting amplifier*

The purpose of the liming amplifier is to amplify the small voltage signal from the TIA so that it reaches the voltage swing required by the clock and data recovery circuit. To meet the overall design goals, there are several design considerations. First of all, given the sensitivity requirement of the overall receiver (to accommodate a photo-detector current as small as 20 μA) and the 600 Ω differential gain of the TIA, the limiting amplifier needs to have a sensitivity of 12 mV_{pp}. The gain of the limiting amplifier should be sufficient to amplify such a small signal to a few hundreds of mV (400mV_{pp} in our design). Second, the minimum overall bandwidth must be 3.5 GHz (5 Gbit/s x 70%) to achieve an overall data rate of 5 Gbit/s [1]. Moreover, the input referred noise of the liming amplifier must be smaller than 857 μV(12 mV_{pp}/14) for a BER of 10^{-12}. Finally, the input capacitance of the liming amplifier must be small so that it does not load the preceding TIA and reduce its performance.

To meet the above design specifications, we designed the liming amplifier using gain stages followed by an output stage to drive a 50 Ω load. The overall architecture of the limiting amplifier along with the TIA is depicted in Figure 4. The number of stages is chosen to be four to keep the overall power dissipation from being too high. To make the input capacitance of the limiting amplifier low while still maintaining a high bandwidth and delivering sufficient current to drive the output stage, we designed the four gain stages with increasing driving capabilities. As shown in Figure 4, each stage is biased with increasing current. To minimize the input referred noise, the first stage (LA1 in the Figure 4) was designed to have higher gain than the following stages so that the noise from stages LA2-LA4 is effectively suppressed. In addition, an offset cancellation circuit is added to prevent the mismatch in the differential gain stages from saturating the gain stages.

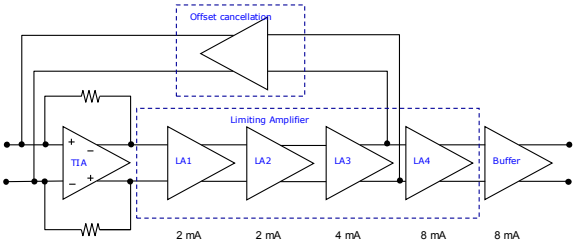

Figure 4 : The overall architecture of the LA

In the following subsections, we will describe the design of each gain stage and the output driver.

B. *The design of the limiting amplifier gain stage*

To achieve a high bandwidth for the overall limiting amplifier, the bandwidth of each gain stage (LA1-LA4) needs to have a substantially higher bandwidth. We adopted the Cherry and Hopper (CH) topology [2] as the base line and employed resistive loading and inductive peaking techniques to further broaden the bandwidth. Figure 5 shows the modified CH stage used in our design. It consists of a tranconductance stage followed by a gain

stage with shunt feedback. This topology guarantees that every node in the CH circuit is low impedance, thus yielding a high bandwidth. The resistive load in the transconductance stage provides a higher bandwidth than a current source load; in addition, an active inductive peaking circuit, made of transistors M6 or M5 and resistors R8 or R7 extends the bandwidth by another 34% over the purely resistive loaded topology.

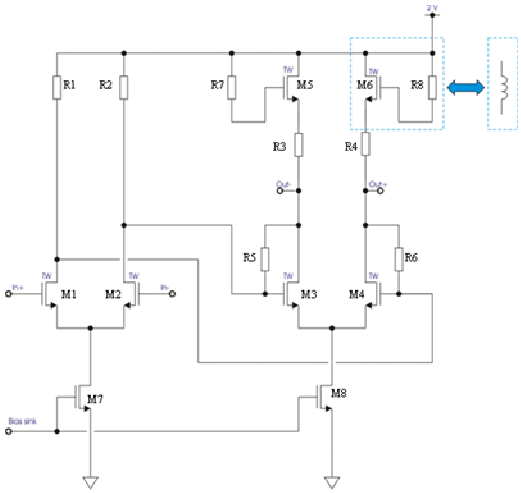

Figure 5 Schematic of one LA stage

C. *The 50 Ω output driver*

To provide a 400 mV_{pp} output voltage, the nominal bias current in the 50 Ω output driver is chosen to be 8 mA (Figure 6). To fully switch the bias current from one arm of the differential pair to the other, the input voltage at the output driver should be large enough. This is only achieved through sufficient gain from the stages of LA1 to LA4.

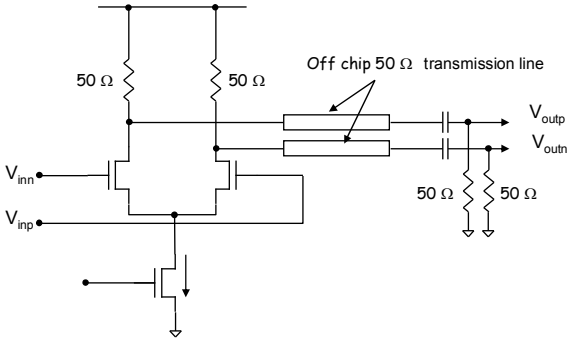

Figure 6 Schematic of the 50 Ω output stage

D. *Simulation Results*

Extensive simulations have been performed on the limiting amplifier to make sure that it works against various process corners, supply voltages and temperature variations. The overall limiting amplifier achieves a gain of 40 dB and a bandwidth of 4.3 GHz in typical cases (TT corner and 27 °C), and a gain of 28 dB and a bandwidth of 3.9 GHz in the worse-case scenario (SS corner and 100 °C). These simulations were done with a double 50 Ω termination as shown in Figure 6. The input referred noise in the worst-case scenario is 309 µV, lower than maximum noise allowed by the design specification.

IV. PIN DIODE BIAS AND LEAKAGE CURRENT EFFECT

The pin diode leakage current increases with the radiation dose level and can reach a value of 1 mA for the dose level expected in the Super LHC upgrade. This current will increase the low cut-off frequency. The proposed biasing for the photodiode in Figure 7 is capable of maintaining this frequency to be lower than 1 MHz and thus be compatible with the GBT encoding.

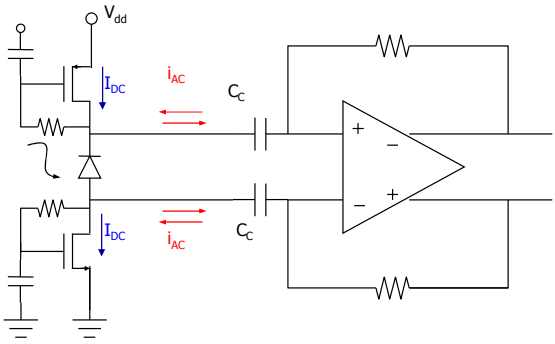

Figure 7 Pin diode bias circuit

Additionally, the leakage current level has an effect on the noise and the sensitivity. In fact when the DC level is around 1 mA, the shot noise becomes comparable to the receiver noise. A sensitivity degradation is thus expected at the end of life of the SLHC. Simulations show a sensitivity loss of 3-4 dB.

V. MEASUREMENT RESULTS

The GBTIA was designed and implemented in a 0.13µm CMOS process. Figure 8 shows the chip photograph where the die size is 0.75 mm × 1.25 mm. The chip is wire-bonded to a high speed photodiode with a responsitivity of 0.9 A/W at a wavelength λ = 1310 nm and parasitic capacitance around 240 fF.

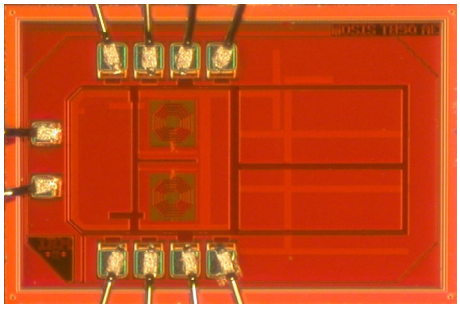

Figure 8 The chip microphotograph

In order to minimize the wire bond effect and particularly the input parasitic capacitance, the connection between the TIA and the pin diode is made very short and does not exceed 200 µm (Figure 9).

The power dissipation of the GBTIA is 120 mW for a power supply of 2.5 V.

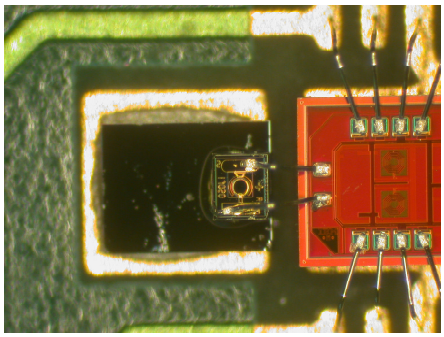

Figure 9 Photodiode to the GBTIA connection

A. *Eye diagram measurements*

The differential eye diagram is measured at 5 Gbit/s and for different optical input levels. The pin diode is illuminated on the top by an optical signal coming from a high speed optical transmitter. Using a PRBS sequence length of 2^7-1, we obtained a clear and well opened eye diagram for an input power of −6 dBm. The eye diagram is still acceptable when the optical input is set to −18 dBm (Figure 10).

For a −6 dBm input, the rise time is 30 ps and the total jitter is maintained below 0.15 Unit Interval (UI) for a bit error rate of 10^{-12}. For a −18 dBm input, the jitter is less than 0.55 UI and the rise time around 60 ps.

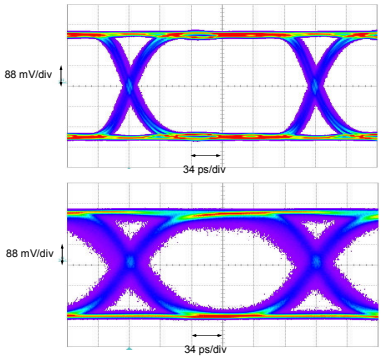

Figure 10 Measured differential eye diagrams at 4.8 Gbit/s (a) −6 dBm input (b) −18 dBm input

B. *BER estimate*

A BER tester based on a commercial 10 Gbits/s optical transmitter and a high performance FPGA was used in order to measure the BER variation with the input optical level at the bit rate of 4.8 Gbit/s. With a PRBS sequence length of 2^7-1, the measured sensitivity is better than −19 dBm for a bit error rate of 10^{-12} (Figure 11).

The output differential output is 400 mV and remains constant even for low optical input levels.

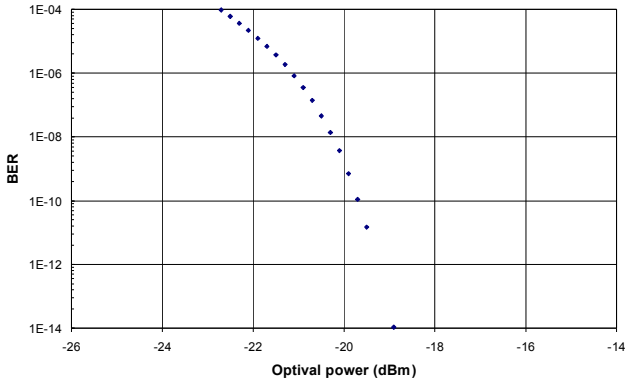

Figure 11 : BER versus the input optical level for 2^7-1 PRBS sequence

C. *BER measurements with the GBT protocol*

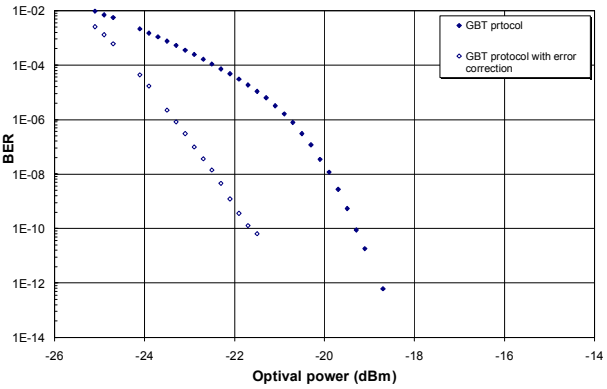

Figure 12 : BER versus optical level for the GBT data encoding sequence

In the GBT chip an error correction system is implemented. This system is based on the Reed-Solomon error-correcting encoder/decoder. Since the Single Event Upsets (SEU) on the photodiodes are considered to be the main source of errors, the proposed line encoding includes an error correction scheme particularly targeted to this issue. Without enabling the error correction system, the sensitivity is around −19 dBm for a BER of 10^{-12}. The sensitivity is improved by 2 dB if the correction encoder is enabled

D. *Total Ionization Dose effects*

In order to facilitate the irradiation test, the pin diode is replaced in this case by a passive network where the input capacitance is set to 500 fF. Irradiation test was done using CERN Xray facility and only the GBTIA chip was placed under the beam. As shown in Figure 13, we did not observe any degradation of the BER even after a dose rate of 200 Mrad.

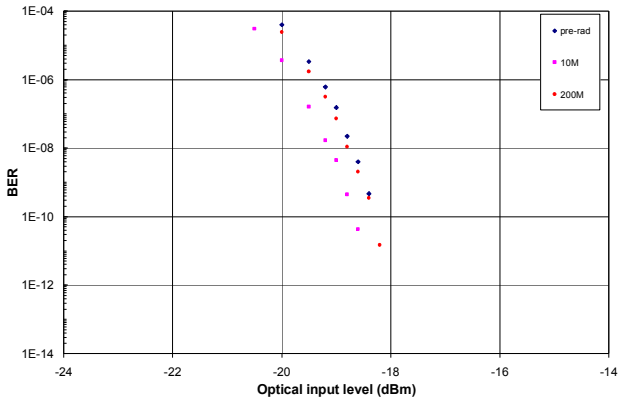

Figure 13 : BER variation with the cumulated dose level

E. Influence of the optical DC level on the BER

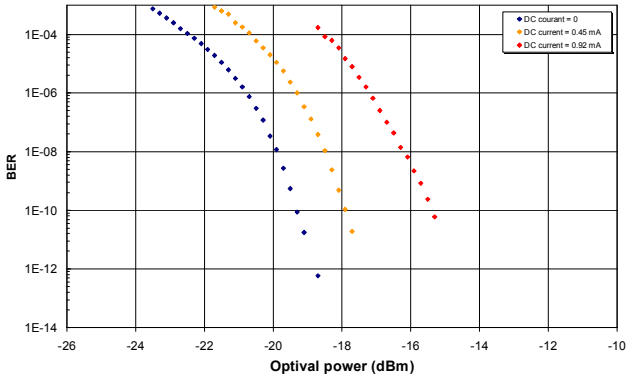

Figure 14 : BER variation with the cumulated dose level

The DC current in the photodiode increases to a value higher than 1 mA after the TID irradiation. In order to measure the influence of this leakage current, the pin diode was illuminated by an additional DC laser source. In this case the integrated bias circuit ensures a sufficient voltage across the pin diode. No noticeable degradation of the BER coming from the effect of the low cut off frequency was observed. The value of this frequency was still compatible with the GBT data encoding when the DC current increased. However, we measured a sensitivity degradation coming from the DC current level. The power penalty introduced by the shot noise of the DC level is around 4 dB as shown in Figure 14.

VI. Conclusion

This paper describes the design of a 5 Gbit/s optical receiver circuit in a 0.13 µm fully CMOS process.

The choice of a differential architecture allows the integration of the TIA and the LA in the same chip and rejects any noise propagated from power supplies.

In order to achieve a high gain, high bandwidth and low noise we used both active and passive shunt peaking techniques in the TIA and LA stages.

The GBTIA has been tested with a high speed photodiode and the most important results are summarized in Table 1.

Table 1 : Summary of performances

Bit rate	5 Gbit/s
Transimpedance gain	20 kΩ
Output voltage	± 0.2 V (50 Ω)
Sensitivity for BER =10^{-12}	–19 dBm
Supply voltage	2.5 V ± 10%
Power consumption	120 mW
Radiation tolerance	> 200 Mrad
Power penalty for high dark current	4 dB

The next step consists of measuring the effects of the Single Event Upset on the receiver and integrating additional features in the final design.

VII. Acknowledgements

We would like to thank L. Amaral, J. Troska and C. Soos from CERN for their help with the test setup and K. Arnaud from CPPM for the test board design.

VIII. References

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