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The GBTIA, a 5 Gbit/s radiation-hard optical receiver for the SLHC upgrades

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This paper presents a 4.8 Gbit/s optical receiver designed in a 0.13 μm CMOS process as part of the GBT project. The receiver consists of a transimpedance amplifier (TIA) and a limiting amplifier. A differential cascode structure with inductive peaking is adopted for the TIA to achieve high gain, high bandwidth and low input referred noise. Experimental results at room temperature show an open eye diagram at 4.8 Gbit/s with rise time < 40 ps, a bandwidth of 4 GHz, and a sensitivity of < -16 dBm for a BER of 10-12. The total chip power consumption is < 120 mW.

Summary

The Gigabit Bi-directional Transceiver (GBT) is a high-speed optical transmission system with a data rate of 4.8 Gbit/s currently under development for HEP applications. This system is intended to be used as bi-directional optical links in radiation environments for the Super LHC upgrade.

At the front end of the GBT chip set is the optical receiver: the GigaBit Transimpedance Amplifier (GBTIA). This paper presents the 4.8 Gbit/s, fully differential, and highly sensitive GBTIA chip designed and implemented in 0.13 μm CMOS process. The chip consists of a low-noise, high-bandwidth transimpedance amplifier (TIA) and a high performances limiting amplifier (LA).

The TIA adopts a differential cascode structure with series inductive peaking to achieve high transimpedance gain, high bandwidth, and low input referred noise. The Photo Detector (PD) current is AC coupled to the TIA using on-chip capacitances. The capacitive coupling rejects the DC current of the PD and allows for a fully differential structure with high power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR). To cope with a potentially high leakage current in the PD induced by radiation, a novel PD biasing circuit is designed in the TIA to ensure the proper biasing of the PD for a leakage current ranging from 1 pA to 1 mA.

The LA is designed with four limiting amplifier stages followed by a 50 ohm output stage to achieve high gain and high bandwidth. Each limiting stage employs a modified Cherry-Hooper structure with resistive loading and active inductive peaking to enhance the bandwidth. The four limiting stages are sized with increasing current and transistor dimensions capable of delivering 8 mA to the output stage while maintaining a high bandwidth.

The GBTIA chip has been tested with a high-frequency PD in the lab at room temperature. The experimental results show an open eye diagram at 4.8 Gbit/s with 40 ps rise time. At 4.8 Gbit/s, the measured sensitivity with 27-1 PRBS is lower than -16 dBm for a BER of 10-12. The chip achieves an overall transimpedance gain of 70 Kohm with a measured bandwidth of 4 GHz. The total power consumption of the chip is less than 120 mW and the chip die size is 0.75 mm x 1.25 mm. Irradiation testing of the chip is currently under way; both pre- and post-irradiation test results will be presented at the conference.

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