OMEGAPIX: 3D IC prototype of the LAL contribution in VITESSE Consortium, dedicated to the ATLAS upgrade SLHC pixel project

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Introduction

The OMEGAPIX circuit is the first front end prototype ASIC designed at LAL using 3D technology for the ATLAS upgrade SLHC pixel project. The microelectronics team from LAL focused its efforts on the specific approach of sub-micron circuit dedicated for innovative high granular planar pixel sensors.
This circuit has been submitted on May 2009. It is build in a two tiers IC stack: one analogue layer and one digital layer. The same 0.13 um Chartered Semiconductor technology has been chosen to design and fabricate the two stacked tiers; the vertically integration process from Tezzaron Semiconductor Corporation performs the wafer thinning and IC bonding.
OMEGAPIX embeds 64x24 readout channels that have been developed to match the following requirements: low noise (100 e-), low threshold (1000 e-), very low power consumption (3 µW/ch) and a very high pixel granularity (50X50 um).
However, the mainly goal of this chip is not to get directly a functional system for the future SLHC planar pixel sensors, but, with requirements close to the likely SLHC ones, we want to explore all features and significant benefits provided by 3D integration technology for HEP and in particular for 3D readout IC system for advanced sensor arrays. To get this, OMEGAPIX has been designed in such a way that various flavours of transistor type will be able to study; the expected reduction of substrate coupling between analogue and digital parts, which is currently the main limitation to low efficiently the pixel signal threshold, will be verified.

VITESSE (Vertical Integrated Technologies for Electronics and Silicon Sensors): a new consortium to explore vertical integration benefits for pixel arrays

What is the 3-dimensional (3D) Integration ?
It is "an emerging, system level integration architecture wherein multiple strata (layers) of planar devices are stacked and interconnected using silicon (or other semiconductor material) vias (TSV) in the Z direction"[1].
Three technical keys are necessary to control this technology: (1) TSV formation, (2) thinning of the wafer up to 12 um thin, (3) Alignment and bonding.
Main benefits: better electrical performance (interconnect delay diminution and better latency), lower noise, form factor improvement (less material, more little device size), more functionality (several technology in the same global device).

Why ? to explore the range of options available and to understand which applications can best benefit from this new technology. The consortium intends to bring together resources to investigate options and share costs.

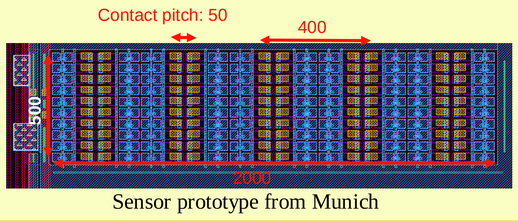
Who ? five IN2P3 institutes (LAL, CPPM, IPHC, LPNHE, CMP), IRFU (CEA-Saclay, France), six Italian institutes (Bergamo, Pavia, Perugia, Bologna, Pisa, Roma), University of Bonn in Germany, AGH university of Science & Technology (Poland), Fermilab (USA)

How ? each institute designs its own 3D chip, then all are gathered in Fermilab.

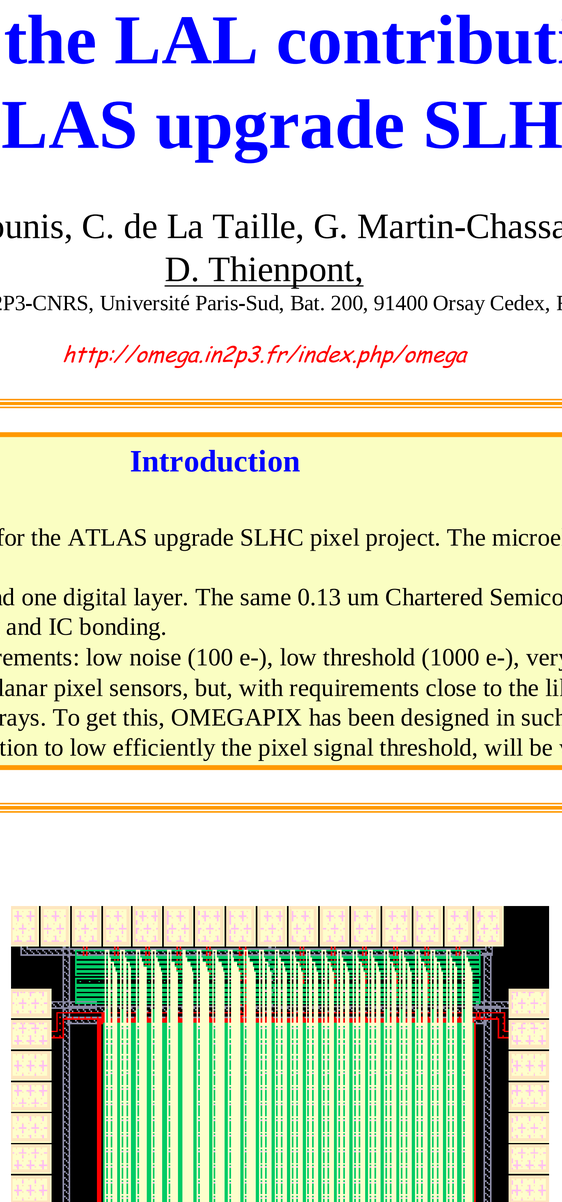
[1]: Handbook of 3D Integration, edited by Philip Garrou, Christopher Bower and Peter Ramm.

SLHC: Small pixels design

Alternative approach use 3D possibilities to:
- ✓ Minimize pixel pitch: study smaller pixels (50x50 µm instead of 50x250)
- ✓ Match new MPI Munich pixel sensor matrix
- ✓ Target 3 µW/ch: 2 µW/ch for the analogue tier, 1 µW/ch for the digital one
- ✓ Design analogue tier with low noise (100 e-) low threshold (1000 e-) low power including shaping + threshold DAC
- ✓ Study coupling between digital tier and analogue tier
- ✓ Study variant of blocks



Sensor prototype from Munich



Chip size

Height= 4.08 mm
Width =1.74 mm
Area = 7.1 mm²
Technology: 0.13 um Chartered
Power Supply: 1V / 1.2 V
Package: CQFP100

Analogue Part

The analogue front-end structure: charge preamplifier, shaper and discriminator.
DAC 5 bits and variable gain (shaper) perform the threshold tuning.

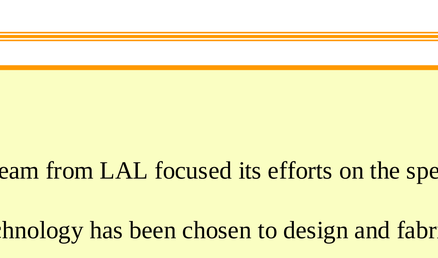
Minimize global capacitance:
- the most little size
- current minimization

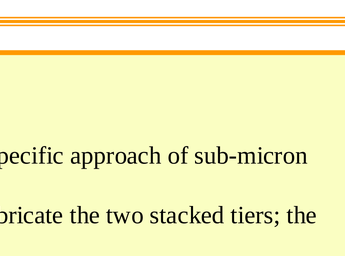
Paraphase structure is described bellow.

Preamplifier

✓ Parasitic capacitance Cgd performs the feedback capacitance: Cf = Cgd ≈ 1,6 fF. Ideal gain is 1/Cf -> 100 mV/ke- (625 mV/fC)

✓ A paraphase structure has been used to fix the DC points, equivalent to a non-inverting CS, transconductance = gm1.gm2/(gm1+gm2) depending of the current





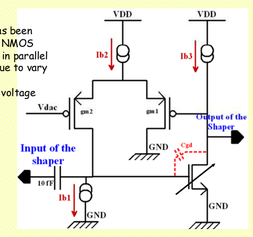
Shaper

Ib1 = 2.5 nA, Ib2 = 5 nA, Ib3 = 50 nA

Basically the same structure than the preamplifier.
Variable gain + DAC 5 bits

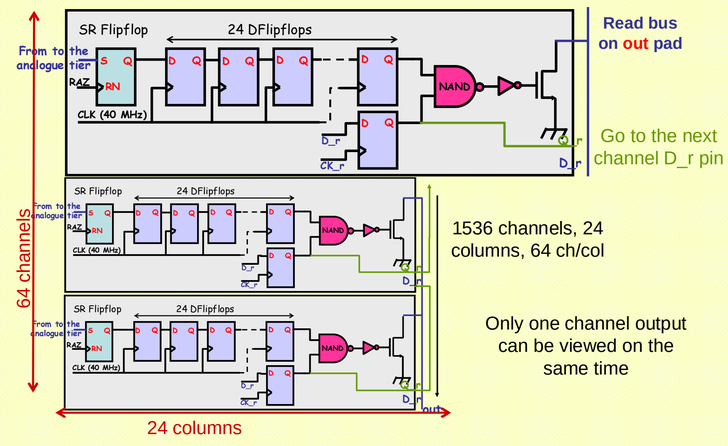
A shaper variable gain has been designed; four different NMOS transistors can be switched in parallel which leads to make Cgd value to vary

DAC fixes the output DC voltage



Digital part

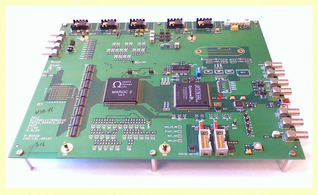
Digital tier has been designed by Yixian Guo from LPNHE. Each channel includes a 24 DFlipflop register: main tests will focus about the noise study

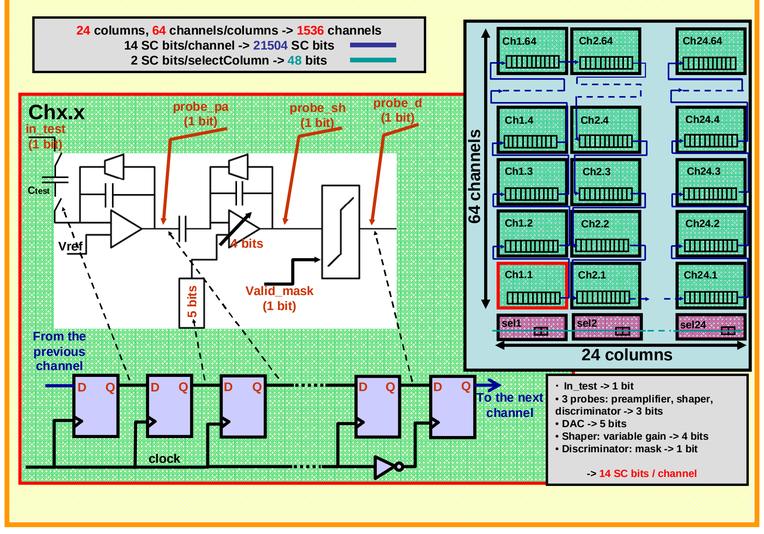


Dedicated test chip

Analogue tier:
-Probes after the preamplifier, the shaper and the discriminator
-Masked discri capability
-Integrated test capacitance
-Bias column selection
⇒different columns: variable components

Digital tier
-1 RS FlipFlop
-24 DFlipFlops
-One global readout
⇒ noise influence studies





Simulation results

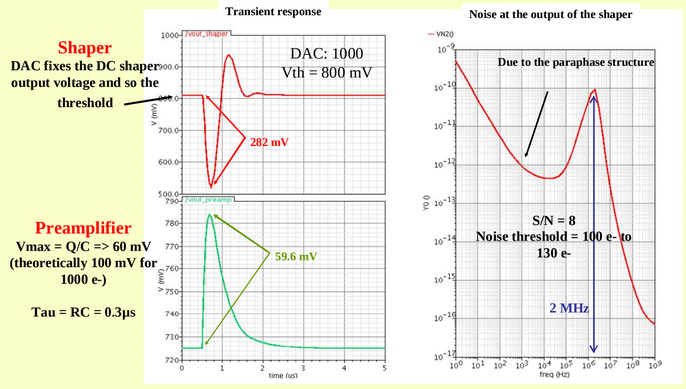
Several column types have been designed allowing us to study various flavors of transistor types (normal, low Vt, 3p3), noise, oscillations…
- ✓Column 1 to 10: reference channels
- ✓Column 11 to 18: various preamplifier transistor types have been integrated
- ✓Column 19 to 22: without variable gain
- ✓Column 23: discriminator has been removed
- ✓Column 24: shaper has been removed

Simulation conditions: Qinj = 1000 e-
DAC: 1000 (only 2.5/0.5 nmos_1p5_lvt as shaper), Vth = 800 mV

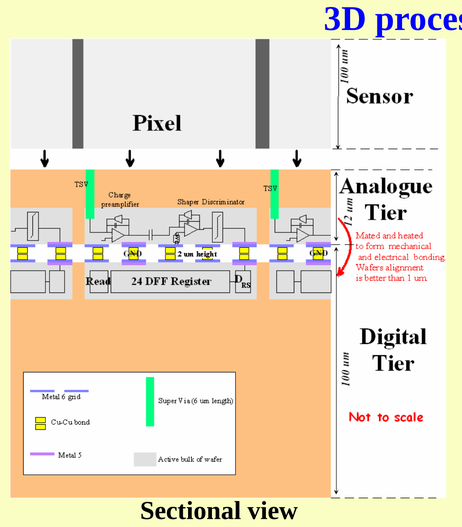
Shaper
DAC fixes the DC shaper output voltage and so the threshold

Preamplifier
Vmax = Q/C => 60 mV (theoretically 100 mV for 1000 e-)

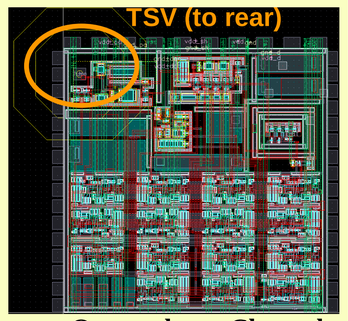
Tau = RC = 0.3µs



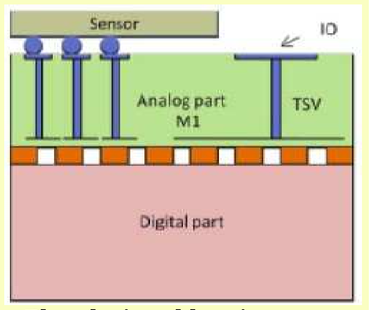
3D process



Sectional view



One analogue Channel



Chartered:
✓ transistor fab,
✓ TSV
✓ Complete back end of line process
Tezzaron
✓ bond two wafers (Cu-Cu thermocompression bond)
✓ thin one wafer up to 12 um to expose TSV
✓ Add metallization on back of this wafer for bump bonding or wire bonding

Place logic, addressing, readout storage, service into another layer: only I/O pads overshoot the sensor plan.

LAL (Laboratoire de l'accélérateur linéaire) is a physics laboratory in Orsay (France), 20 km away from Paris. 350 people including around 100 physicists work on many experiments in cosmology, high energy particle physics and accelerator. Several technology groups such as the mechanics or the electronics group work on applications to achieve physicists expectations.

The LAL electronics group (50 people) is divided in 3 units : digital design unit, analog design unit, and automated equipment design unit. Teams are involved in many large physics experiments such as Atlas, Planck, Auger and FLC. The group can work on project from the manufacturing standard to the production and ensure maintenance.

The analog team has acquired a sharp knowledge in full-custom analog ASIC design. Its specialization is focused on low-noise high-speed front-end chip and on high-precision calibration devices. Its know-how is evolving to system-on-chip designs that embed front-end electronic, auto-trigger system, calibration devices and digital converters.

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