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OMEGAPIX : 3D electronics chip for pixel readout

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The OMEGAPIX circuit is the first front end prototype ASIC designed at LAL (Orsay) using 3D technology for the ATLAS upgrade SLHC pixel project. This work has been done inside a new international consortium for development of Vertical Integrated Technologies for Electronics and Silicon SEnsors (VITESSE), which has gathered, not only 3 IN2P3 (France) institutes, but also Fermilab (USA) and INFN (Italy) HEP laboratories . One goal of the consortium is to explore the range of design options available that could fit the physics requirement of future high energy colliders.
LAL focused its efforts on the specific approach of sub-micron readout circuit dedicated for innovative high granular planar pixel sensors for Atlas upgrade pixel detector.
This circuit has been submitted on May 2009. It is build in a two tier IC stacks: one analogue layer and one digital layer. For the manufacturing of the 2D part, it has been realized in 0.13um Chartered technology. For the 3D part the Tezzaron process has been used. The process is wafer to wafer technology, face to face, via first and uses Copper-Copper bonds. The circuit embeds 64x24 readout channels that have been developed to match the following requirements : low noise (100 e-), low threshold (1000 e-), very low power consumption (3 uW/ch) and a high granularity (50x50 um). This electronics chip will also allow us to study various flavours of transistors types (normal, low VT, 3p3) and their behaviour when exposed at high radiation levels compatible with SLHC doses.
One other expected improvement of the 3D technology that will be checked is the reduction of substrate coupling between analogue and digital parts and thus should allow us to lower efficiently the pixel signal threshold.
To reach these requirements, a simplified common source configuration has been designed to perform the charge preamplifier and the shaper. A special care has been taken for the minimization of the global capacitance, and, for the shaper, a variable gain and a DC level adjustment have been designed. Design considerations, simulation and hopefully first tests results will be presented.

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