Medipix3 Irradiation Studies

Irradiation Studies of a 130nm Large Area Pixel Chip

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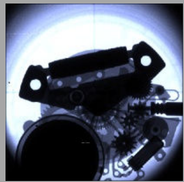


Overview

Introducing the Medipix3 Chip

- Updates from Medipix2
- Charge Summation
- Spectroscopic mode
- Example Application

Brief Radiation Damage Overview

Specific Design Issues

Irradiation Measurements up to 460Mrad

- Threshold, Noise and Gain Results
- DAC Stability

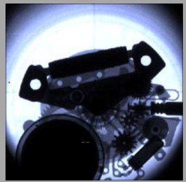
Irradiation Measurements up to 3Mrad

- Additional Run in the Worst Case

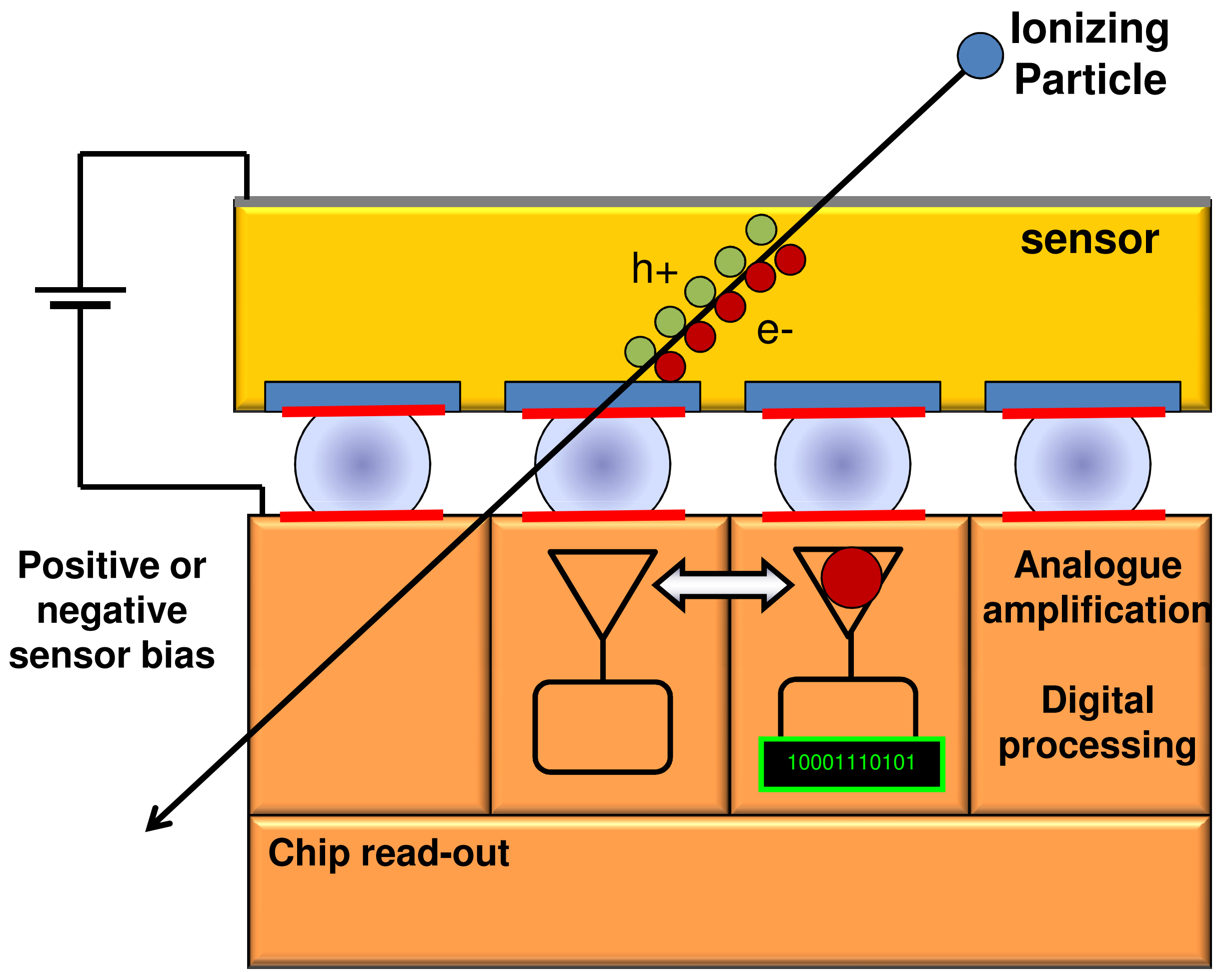
The Medipix3 Design team is Xavier Llopart, Rafael Ballabriga & Winnie Wong

These Measurements taken and analysed by myself, Xavier Llopart & Rafael Ballabriga

Thanks to them and all the CERN group for their support



Hybrid Pixel Detectors



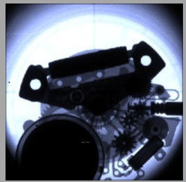
A hit in the sensor deposits charge

The charge passes to the analogue amplifiers

The Medipix 3 charge summing circuit operates

The counter is iterated and read out with the shutter

Medipix3 adds communication between the pixel analogue electronics

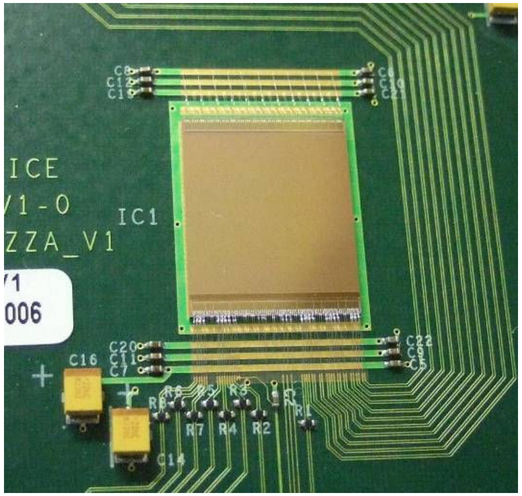


Imaging by Photon Counting

- **Application of HEP idea to x-ray detection and medical imaging, the concept behind Medipix chips.**
- **Photon counting devices provide superior contrast and dynamic range to charge integrating devices.**
- **Counting only hits that pass threshold rejects noise in the sensor giving clearer images.**
- **Dynamic range is limited only by front end response and depth of in-pixel counters.**

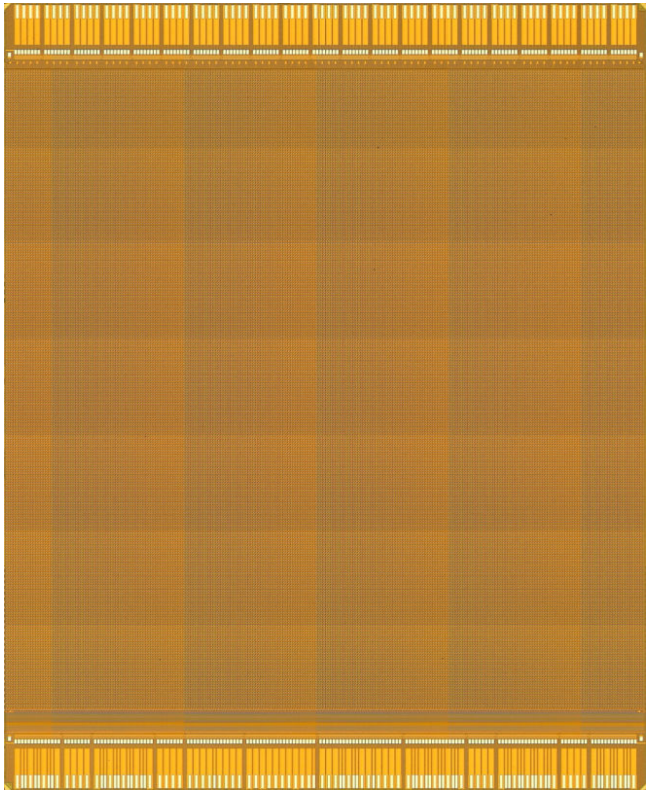
Medipix 3

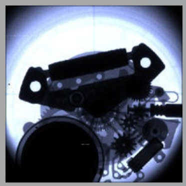
- **Medipix3 builds on the success of Medipix2 as a single photon counting imaging chip**
- **Added Features**
  - **Analogue charge summing to keep all charge information**
  - **Spectroscopic mode with 8 threshold levels**
  - **Continuous readout mode (no dead time)**
  - **Increased counter depth increasing dynamic range**
  - **Increased readout speed**
  - **Increased radiation hardness from 130nm CMOS process**



Status

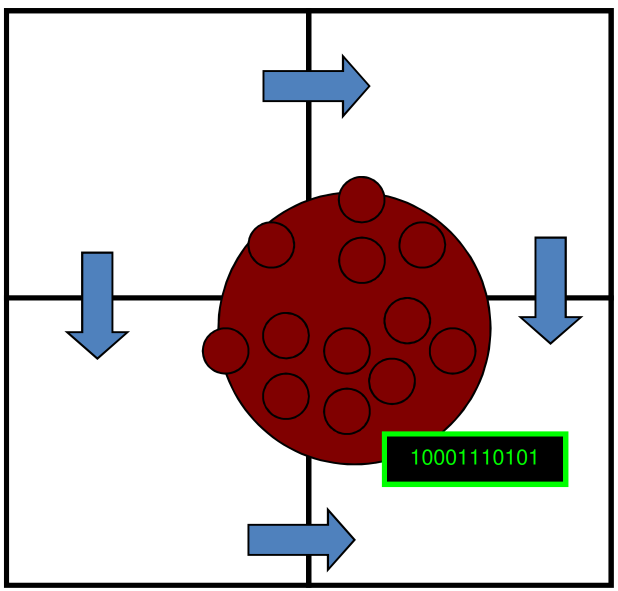
- First engineering run (12 wafers of 100 chips) delivered early this year
- Wafer probing complete (from 11 wafers – 437 Class A + 166 ClassB)
- Initial readout system working at low speed
- Initial characterisation underway
- One wafer diced and bonded to PCBs
- First bump bonded assemblies with wafers expected soon
- Initial radiation hardness measurements underway





Charge Summing

Medipix3 can be set to sum charge across four pixel clusters to prevent hits being lost due to charge sharing



A hit in the sensor deposits charge across four pixels

The analogue comparators assign the charge to the pixel with the most hits

This prevents ‘lost’ charge by partial hits not passing threshold

The threshold is applied to the summed charge and read out when the shutter closes

Spectroscopic Mode

Introduction to Medipix3

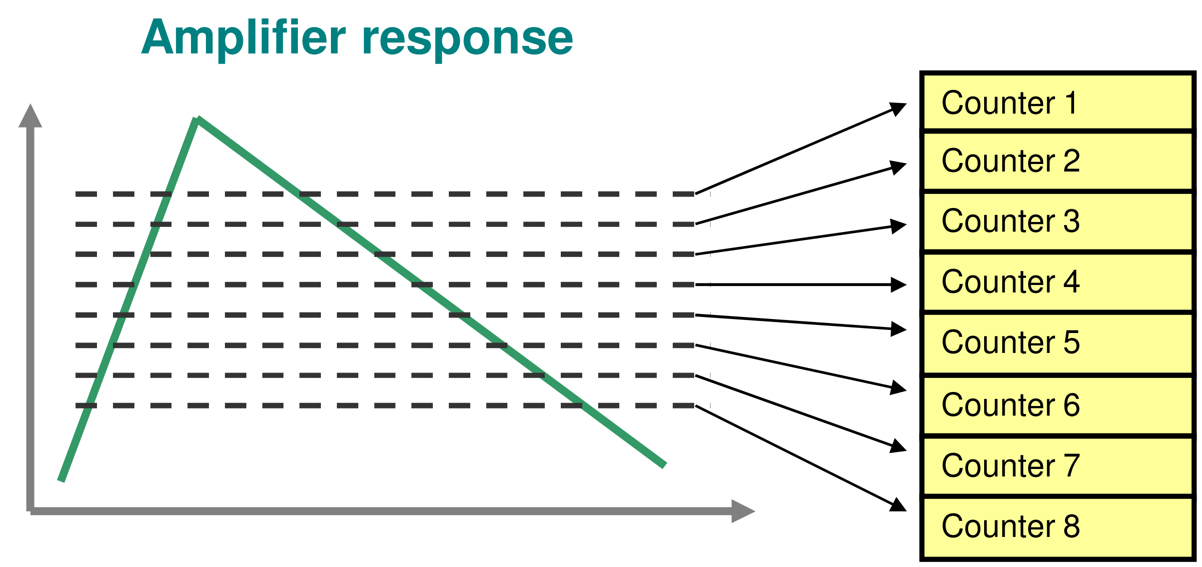
Radiation Damage

Design Issues

460MRad Irradiation

3MRad Irradiation

- By connecting 4 pixels into a larger super pixel, eight threshold levels are available to us in the digital part of the pixel…



- Each threshold is adjustable, allowing a wide range of settings.

- This gives us enough flexibility to capture reasonable spectra in many different applications

MARS Computed Tomography System

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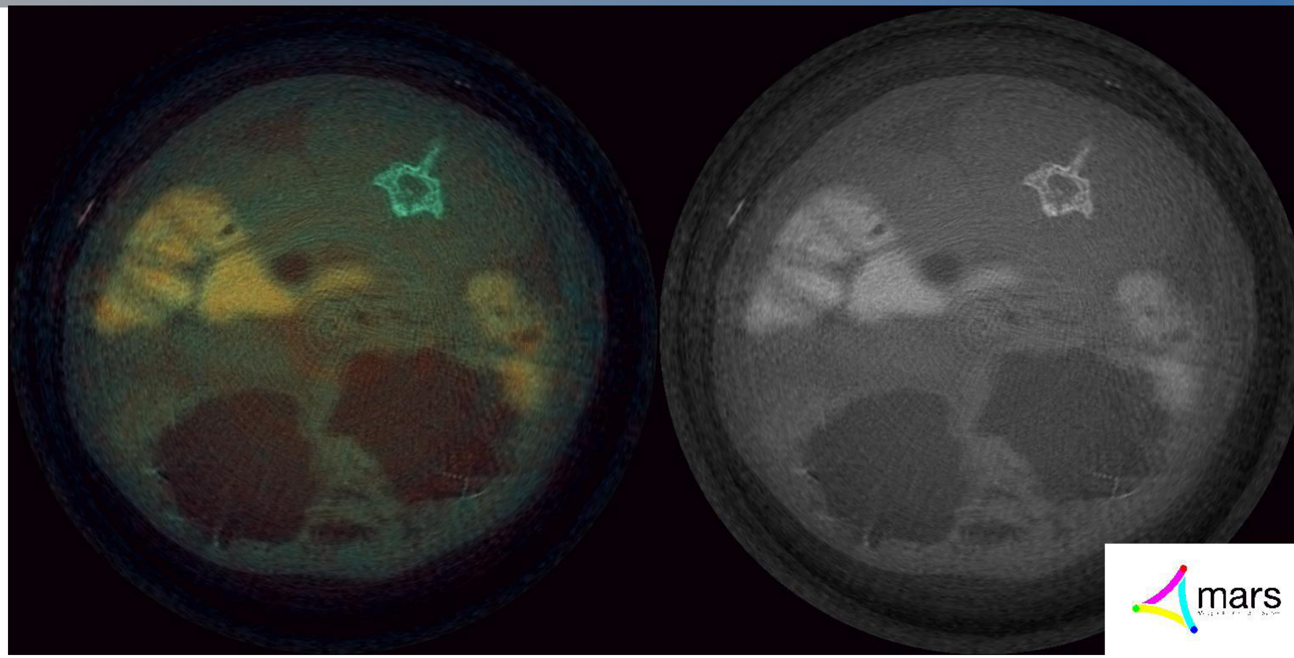
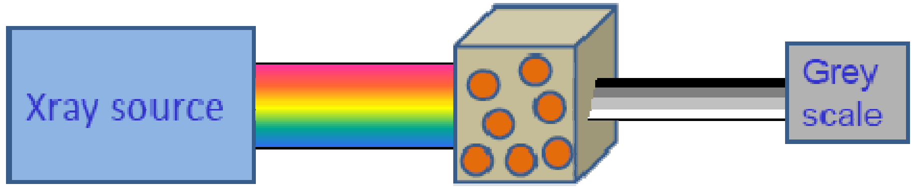
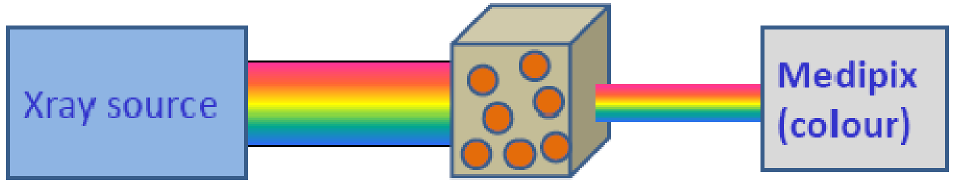
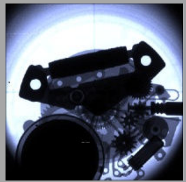


Standard CT



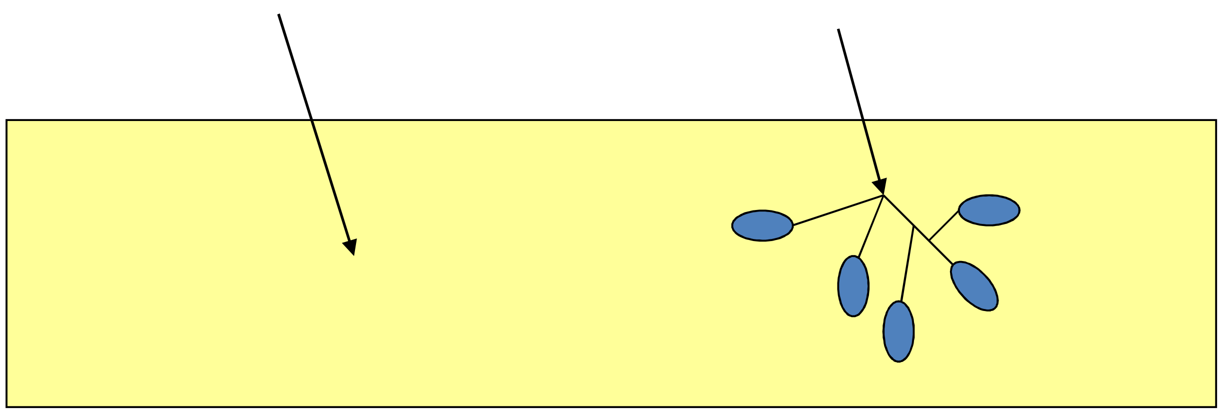
MARS-CT





Radiation Damage

- **130nm is expected to be significantly more radiation hard than 250nm CMOS because of the much thinner gate oxides**
- **Radiation damage occurs because the regular crystal structure of a device is disturbed. This causes a number of effects among which are:**
  - **Change of effective doping concentration (esp. in diodes)**
  - **Increase leakage current (esp. in detectors)**
  - **Charge trapping (esp. in detectors)**
  - **Oxide charging (esp. in CMOS)**
  - **Single Event Upset (in logic circuits)**
- **Photons and hadrons cause different types of damage, point and cluster respectively.**



Analogue Switch Problem

Introduction to Medipix3

Radiation Damage

Design Issues

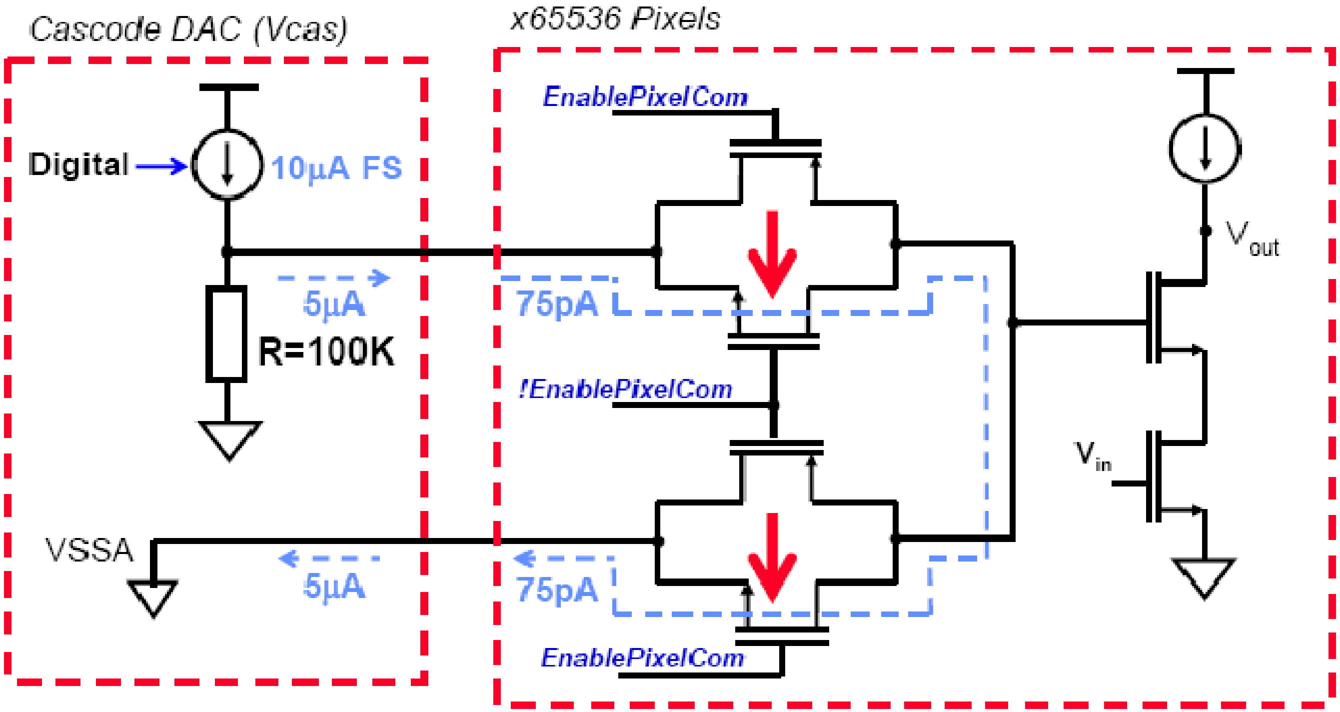
460MRad Irradiation

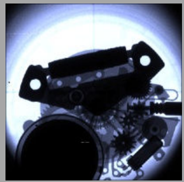
3MRad Irradiation

One of the DAC outputs is particularly sensitive due to a minor design oversight

The current drawn by some minimum sized NMOS transistors when the matrix is irradiated can overload the DAC output stage stopping the pixel front end from functioning under nominal bias conditions

Here it happened at less than 1MRad so we were able to take no proper front end measurements during the 400MRad irradiation





Solution

- **The chip operation can be recovered by modifying the DAC settings.**
- **In particular the pre-amp reference voltage was reduced modifying the front-end operating point.**
- **Next wafer production fix Cas DAC issue by eliminating the (unneeded) leaky NMOS**

400Mrad Irradiation

Introduction to Medipix3
Radiation Damage
Design Issues
460MRad Irradiation
3MRad Irradiation

- **Used a calibrated X-ray machine (Seifert RP149)**
- **Beam profile is smaller than the Medipix3 → Two runs:**

On the Pixel Matrix 60Mrad

Threshold Variation

Gain Variation

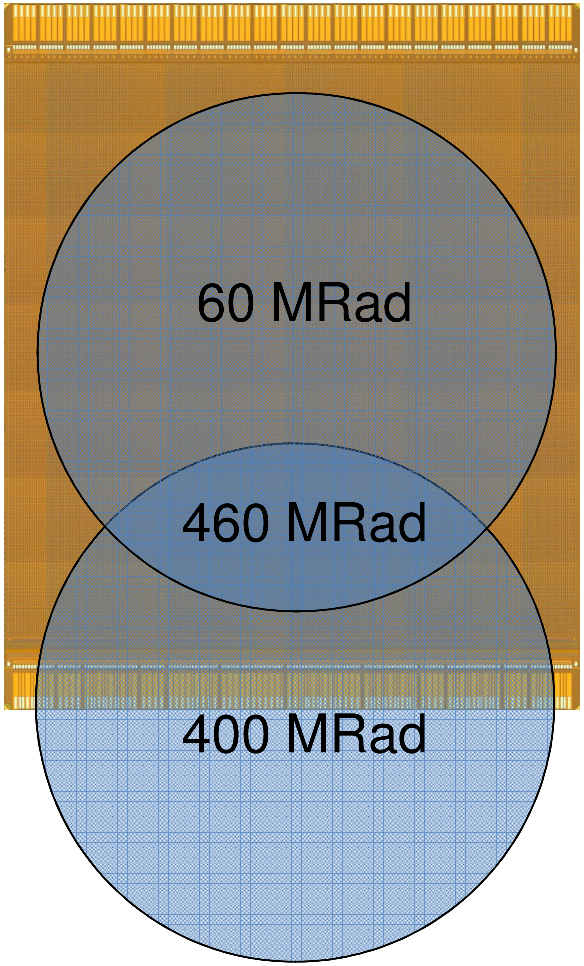
Noise Increase

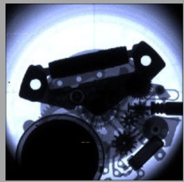
On the Periphery 400Mrad

Check DACs

E-fuses

Logic functionality





Performance after 460MRad

Introduction to Medipix3

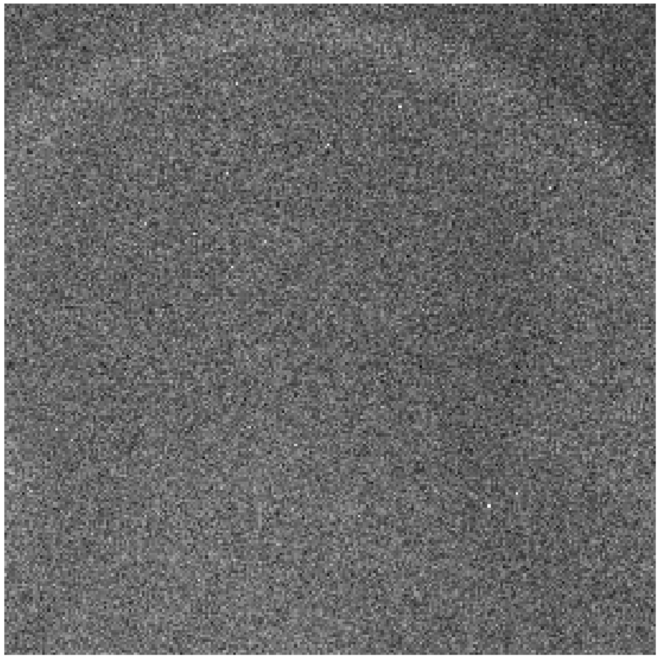
Radiation Damage

Design Issues

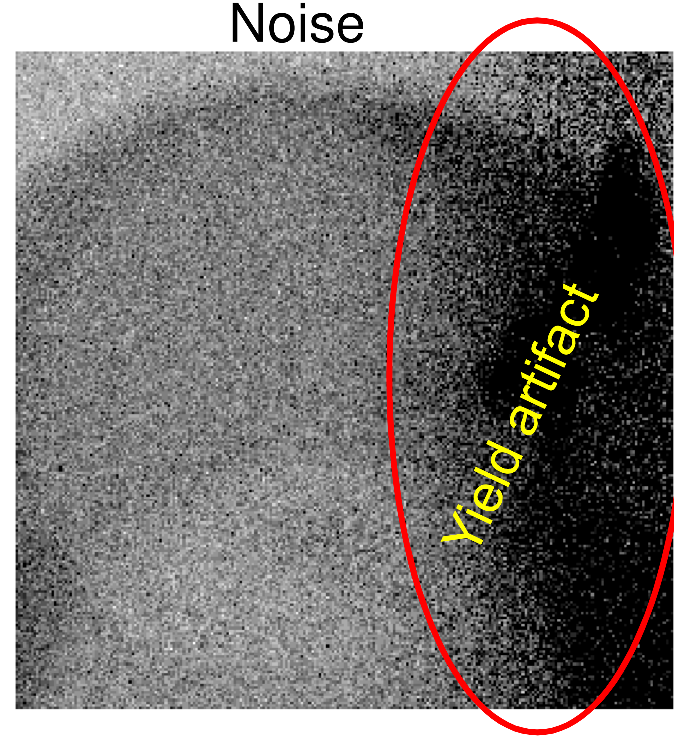
460MRad Irradiation

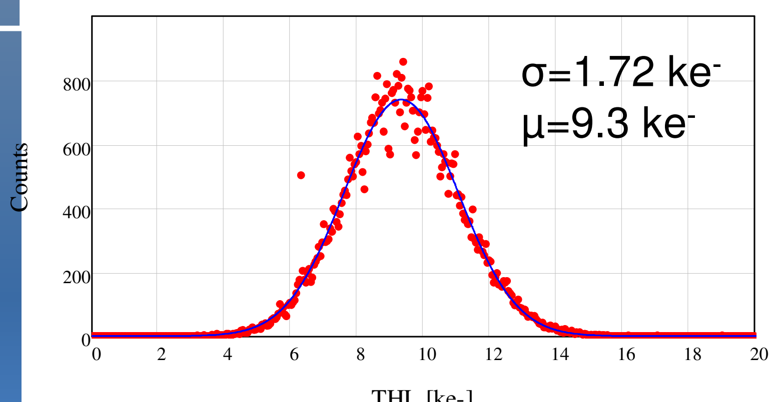
3MRad Irradiation

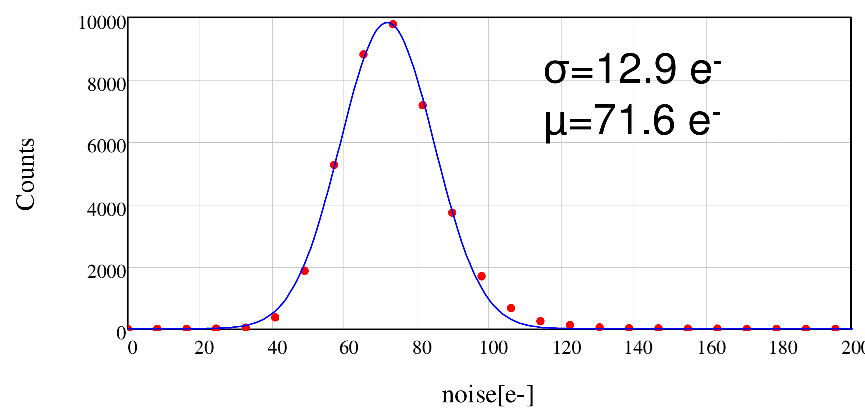
Threshold



Noise

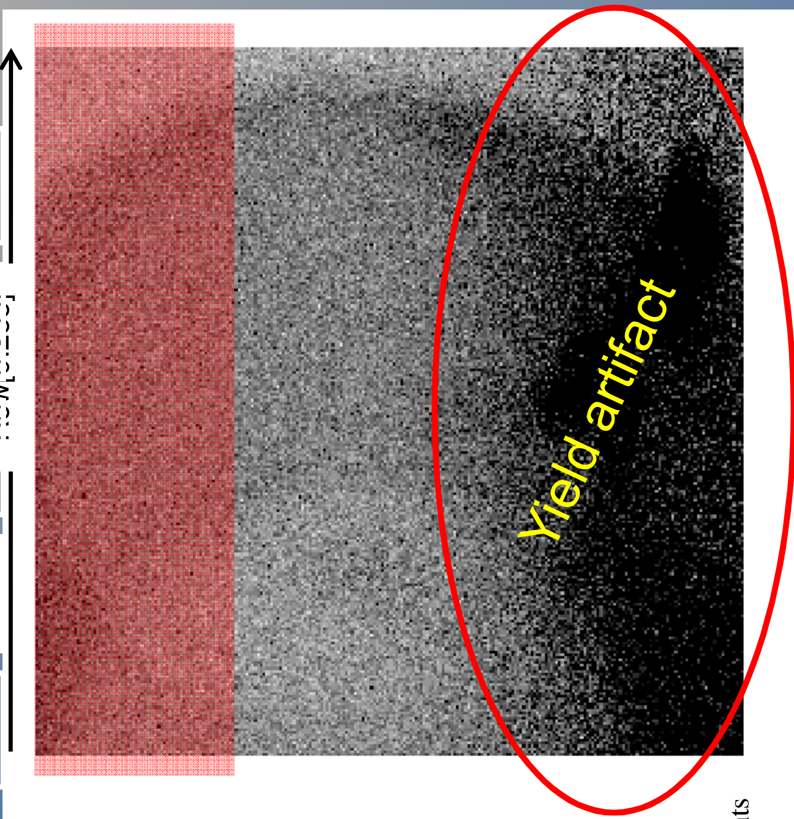


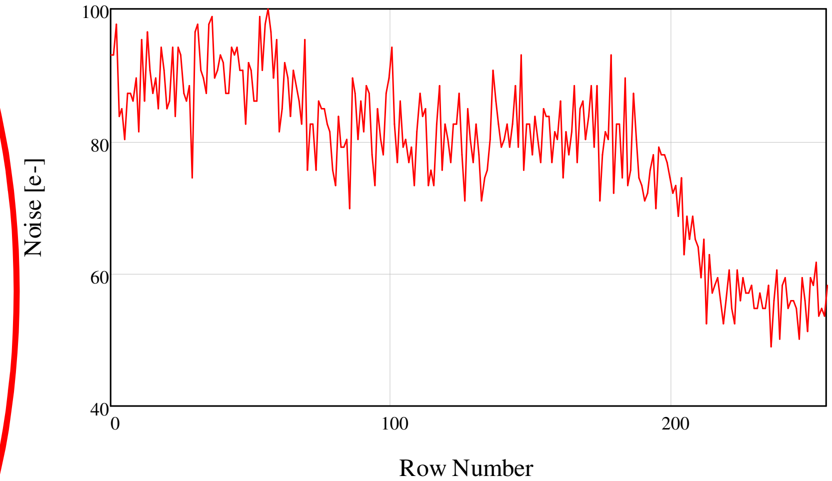


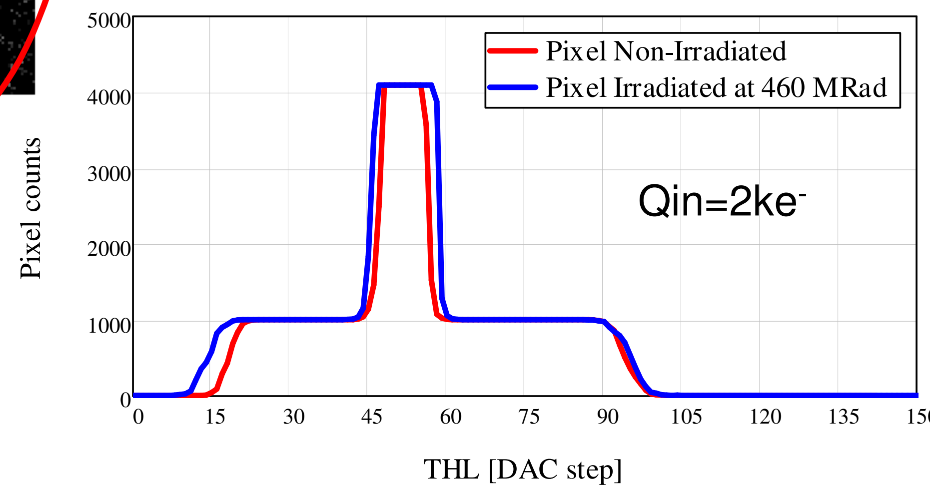


Threshold can be re-tuned using 5 bit equalisation

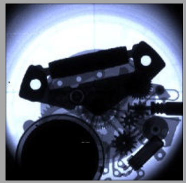
Performance after 460MRad



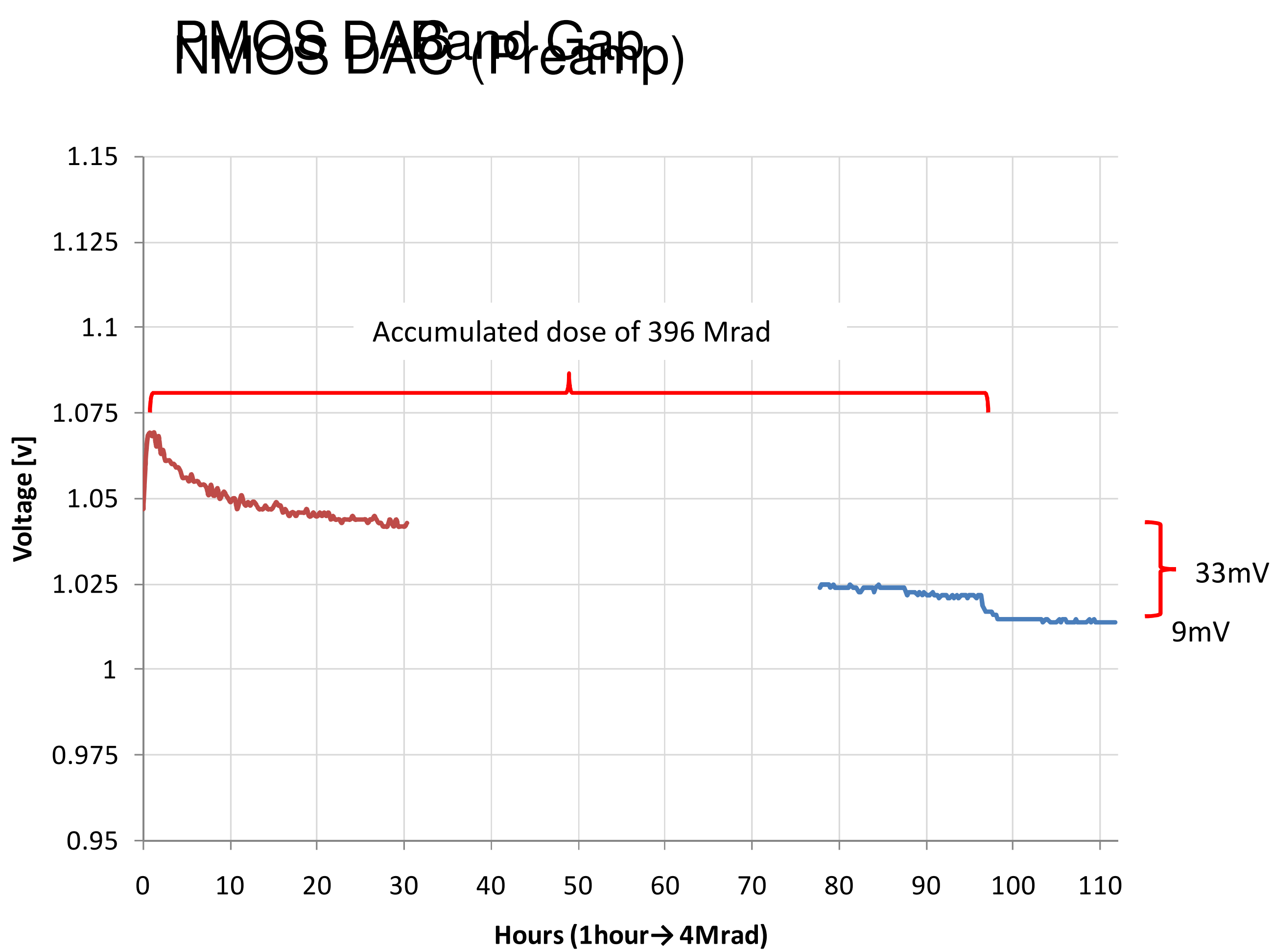




After 460MRad there is essentially no gain variation observed



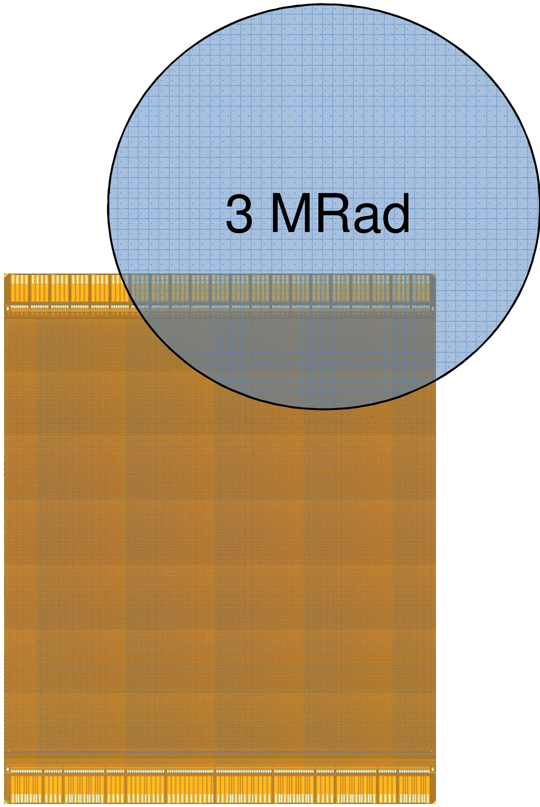
DAC Measurement



3MRad irradiation

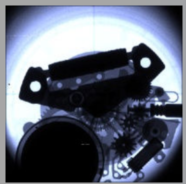
Worst effect at 3MRad, After this the effect of further radiation is much less.

Irradiated a small area of the chip up to 3Mrad to try and keep Cas DAC working by only damaging a limited number of pixels



The main effect observed is the shift in the threshold and amplifier response caused by the DAC moving…

The front end leaves its normal operating point at nominal bias conditions at 1500krad, although it remains possible to read out the chip up to 3Mrad. The front end can be recovered by increasing the value of the IKRUM DAC.



3MRad Noise and Gain Result

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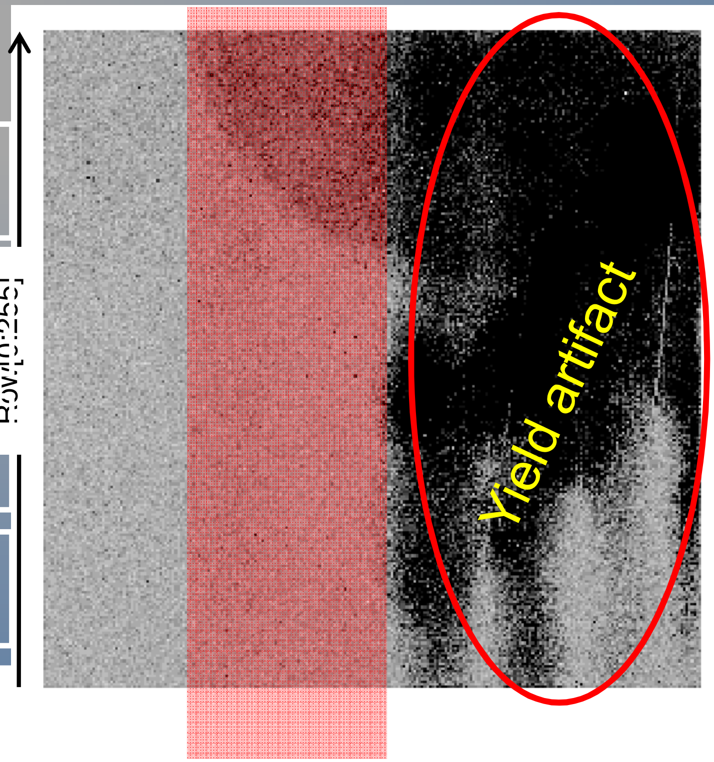
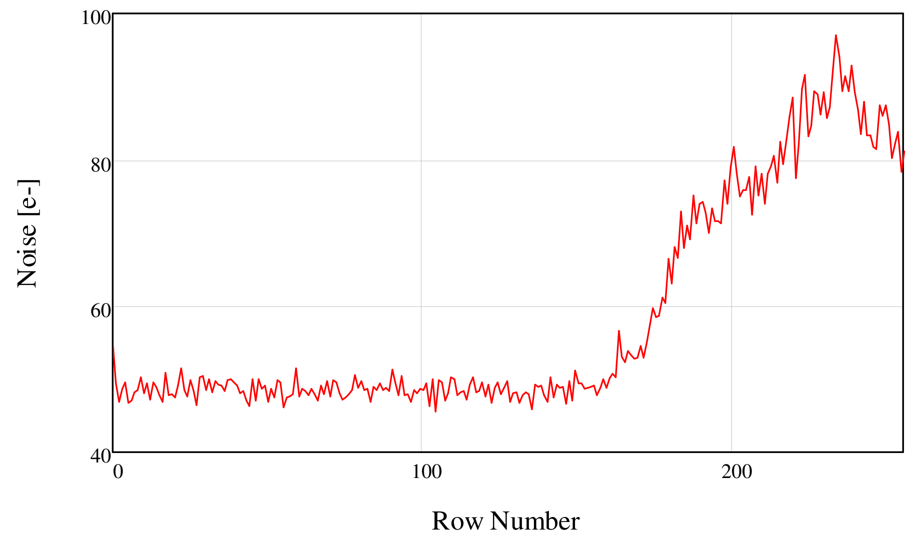
Radiation Damage

Design Issues

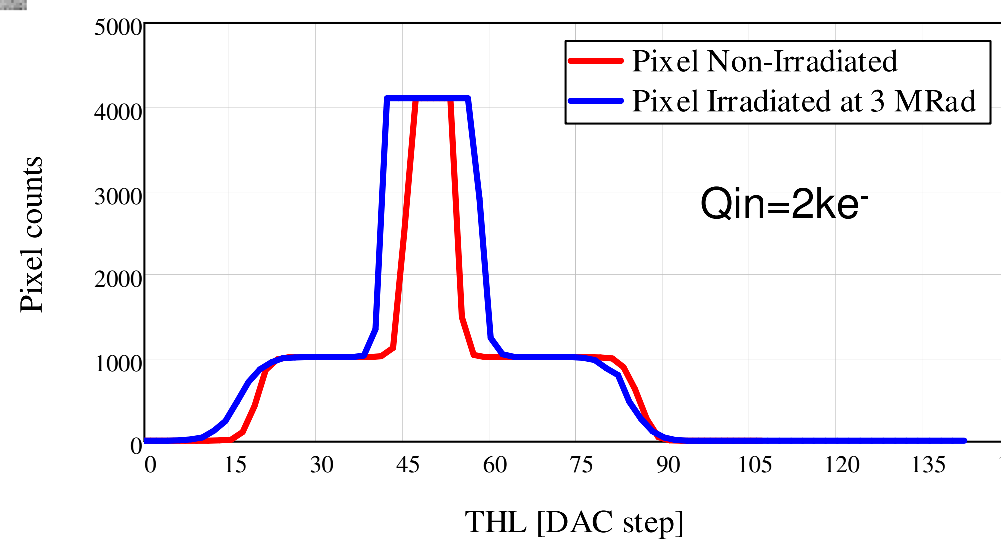
460MRad Irradiation

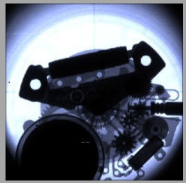
3MRad Irradiation





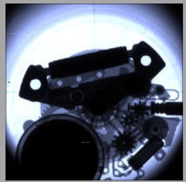
In this worst case situation the noise is still less than 100e$^-$ and the gain variation is still minimal





Next Steps

- **Repeat 400MRad measurement with bare chips and full sensors, recovering performance at each point to take measurements.**
- **Begin hadronic measurements rather than x-rays, possibly in collaboration with LHCb upgrade projects.**
- **Measurements with different sensors eg 3D or diamond**
- **Next wafer production to fix Cas DAC issue by eliminating the (unneeded) leaky NMOS**



Conclusions

- **Medipix3 has been operated successfully after an exposure to a very large x-ray dose.**
- **This is very encouraging for readout chips in SLHC trackers and other high radiation environments.**
- **Confirmation in a full chip that 130nm is intrinsically more radiation tolerant than 250nm.**
- **You still need to bear radiation damage in mind when designing chips to avoid unexpected problems.**
- **Thank you for your attention.**

Backup Slides

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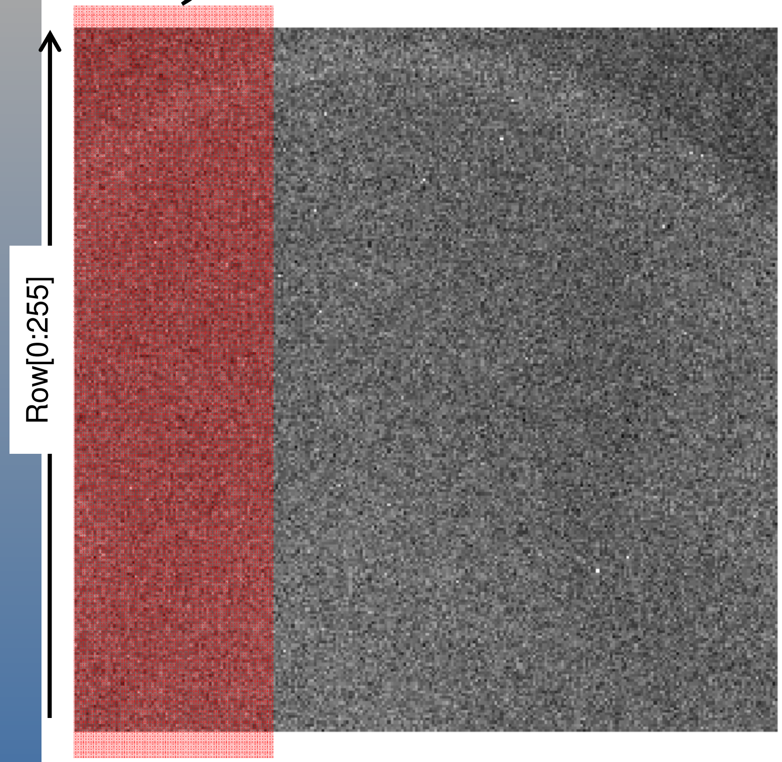
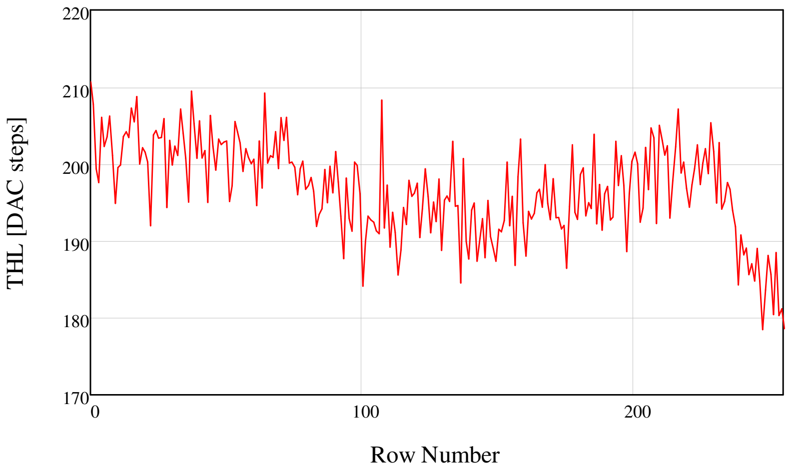
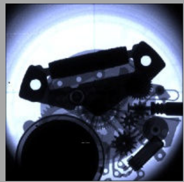
460MRad Threshold variation





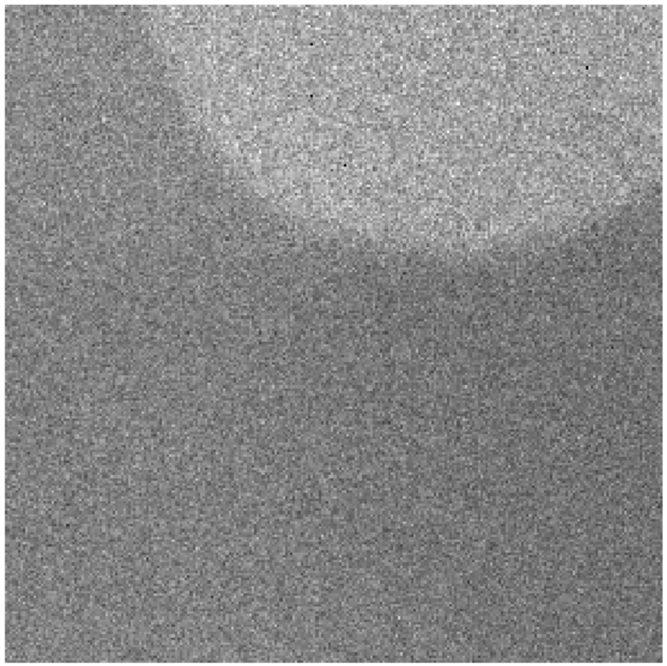
After annealing we see ~20 THL DAC steps variation (<1ke$^-$) between areas non irradiated and areas irradiated at 60, 400 and 460 Mrad.

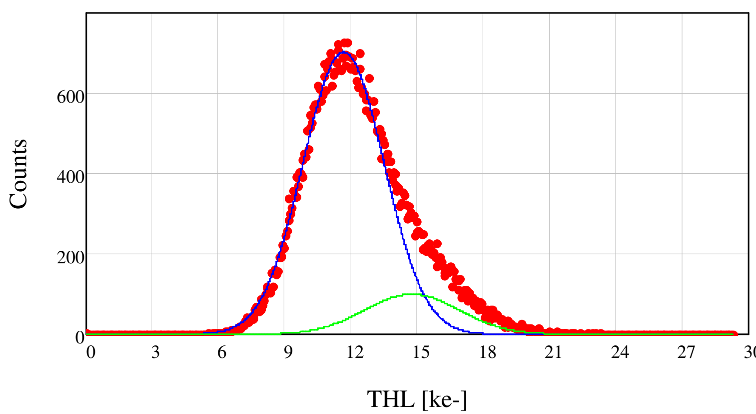
This variation can be corrected by the threshold equalization procedure (5 bits)



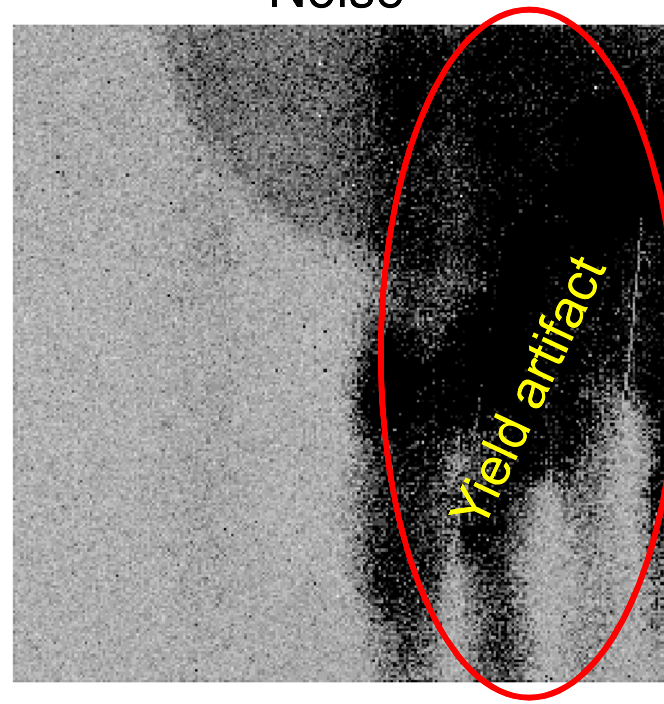
General behavior after 3 Mrad

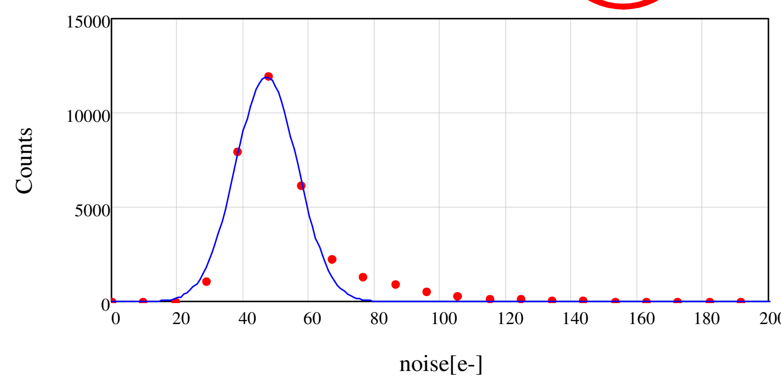
Threshold



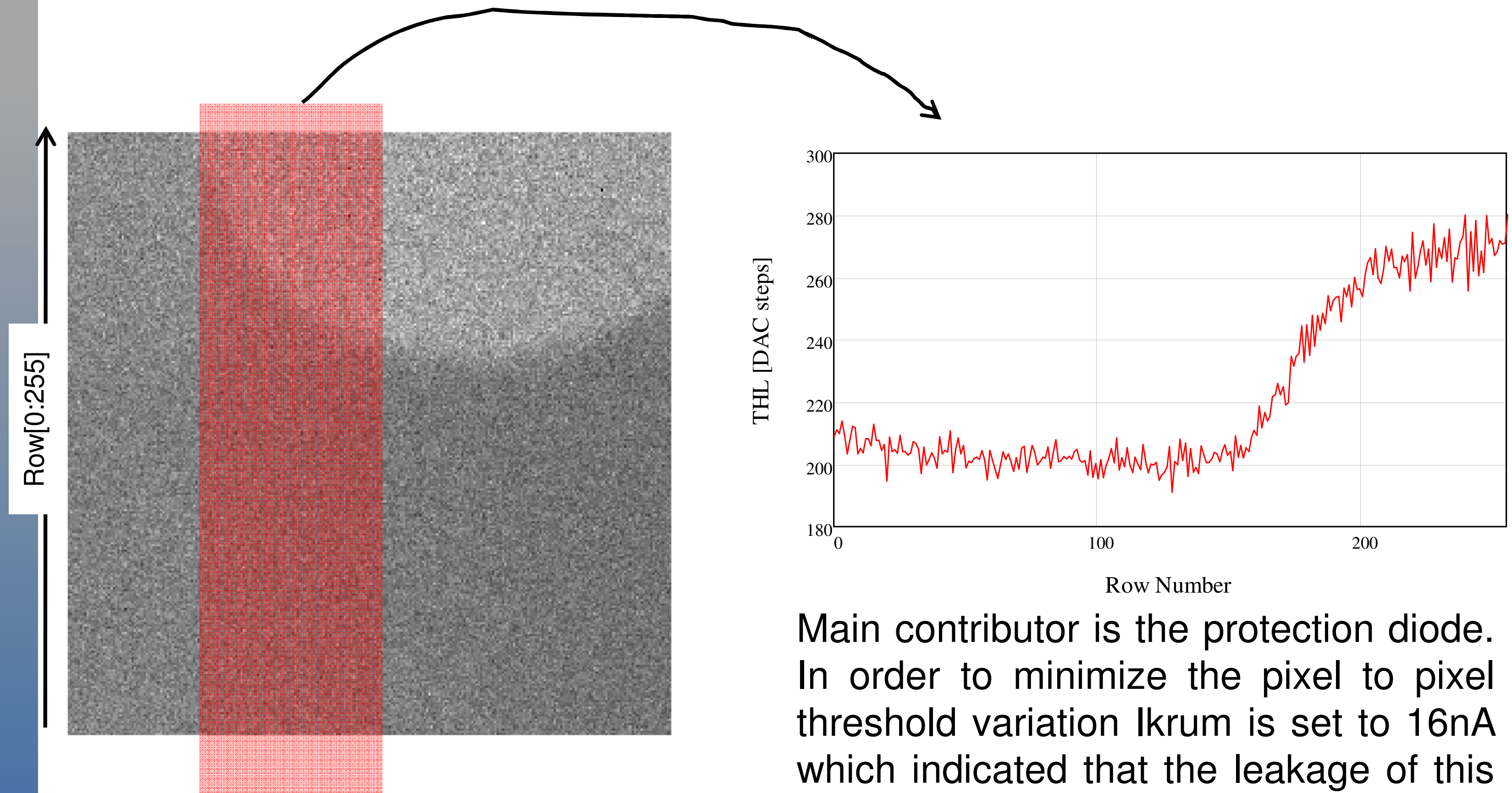


Noise





THL Shift at 3MRad



Main contributor is the protection diode. In order to minimize the pixel to pixel threshold variation Ikrum is set to 16nA which indicated that the leakage of this diode at 3Mrad is ~5 to 10 nA.

This is the worst radiation operation point.

Difference in CAS DAC range

- **Good chip (F7) shows CAS DAC dynamic ranger larger than other chips → Less *ids* transistor leakage in analog switches?**