Contribution ID: **124** Type: **Oral**

Measurement of radiation damage of 130nm hybrid pixel detector readout chips

Tuesday, 22 September 2009 16:40 (25 minutes)

We present the first measurements of the performance of the Medipix3 hybrid pixel readout chip after exposure to significant x-ray flux. Specifically the changes in performance of the mixed mode pixel architecture, the digital periphery, digital to analogue converters and the e-fuse technology were characterised. A high intensity, calibrated x-ray source was used to incrementally irradiate the separate regions of the detector whilst it was powered. This is the first total ionizing dose study of a large area pixel detector fabricated using the 130nm CMOS technology.

Summary

The Medipix3 hybrid pixel detector readout chip is the first 130nm CMOS large area pixel detector to be fabricated. It is expected that the SLHC generation of pixel detectors will use 130nm or 90nm technology, both of which are expected to be significantly more radiation tolerant than the current generation of sensors using 250nm CMOS. This expectation is based largely upon the use of a significantly thinner oxide layer in the 130nm devices and some preliminary evaluation of individual components [1]. It is hoped that these measurements will confirm this intrinsic improvement in a complete large area device, rather than small test structures.
The study will include measurements of the evolution of the performance of the pixel architecture, the digital to analogue converters (DACs) in the chip's periphery, the custom LVDS drivers used to read out the chip and the e-fuse logic that sets the chip's identification number. The tests on the pixel region will concentrate on threshold scans of an injected test pulse and of the noise level. This will yield information on the gain variation of the pixels after irradiation and the position and extent of the noise within the chip. The linearity of the DACs within the chip's periphery will be measured to check for any drift with irradiation. The operability of the chip's digital periphery including its IO logic and LVDS drivers will be checked continuously throughout the studies to give an indication of the point of failure. In addition the e-fuses that set the chips identity code will be read continuously to confirm their survivability. Changes in power consumption of the chip as it is irradiated will also be monitored.
As there are only a very limited number of Medipix3 chips currently available these initial tests will be performed on a single chip, incrementally irradiating a region of the pixel matrix and then the periphery. As Medipix3 has been designed primarily for x-ray imaging in medical applications, it uses mainly the standard 'open'gate transistors and has no features to combat single event upsets (SEUs). For this reason the study will concentrate on the total ionizing dose rather than the SEU cross section. A demonstration of the intrinsic radiation hardness of this technology has some significant implications for the design of future chips for use in HEP, synchrotrons and beyond.

[1] F. Faccio, "Radiation issues in the new generation of high energy physics experiments,"Int. J. High Speed Electron. Syst., vol. 14, pp. 379-399, 2004.Power consumption

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Session Classification: Parallel session B2b - Radiation tolerant components and systems

Track Classification: Radiation tolerant components and systems