Design and measurements of 10 bit pipeline ADC for the Luminosity Detector at ILC

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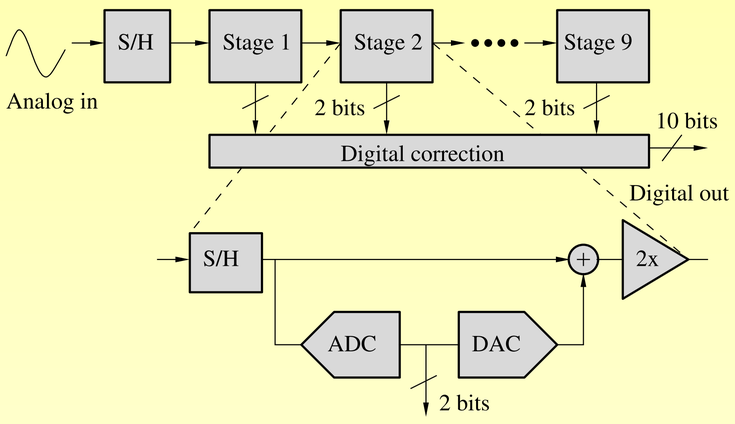
Introduction

The luminosity detector (LumiCal) [1] at the future International Linear Collider (ILC) will need a dedicated multichannel readout [2, 3]. The energy deposited in a sensor, detected and amplified in the front-end electronics, needs to be digitized and registered for further analysis. Considering the number of detector channels needed (∼200,000) and the limitations on area and power, the optimum choice for the analog to digital conversion seems a dedicated multichannel ADC.
The design and preliminary measurements of a prototype 10 bit pipeline ADC based on 1.5-bit per stage architecture are discussed. The ADC was designed in two versions with and without sample-and-hold circuit (S/H) at the input. The prototype is fabricated in 0.35 μm CMOS technology. A dedicated test setup with a fast FPGA based data acquisition system (DAQ) developed for ADC testing is described. Wide spectrum of measurements of static (INL, DNL) and dynamic (SFDR, SNHR, THD) parameters performed to understand and quantify the circuit performance is presented.

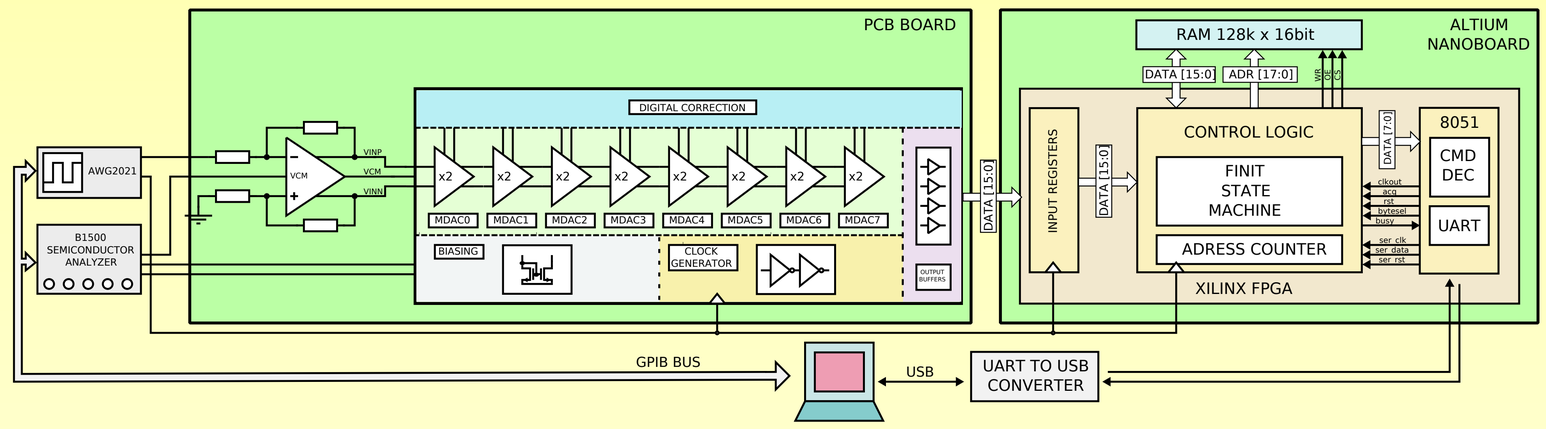
Design



Main features:

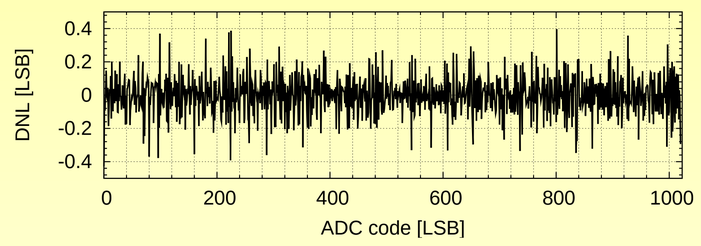
- resulution 10 bit
- sampling frequency up to 30 MHz
- internal switches for clock & power ON/OFF
- fully differential telescopic amplifier with boosted gain and continous feedback
- dynamic latched comparators
- two prototypes with & without S/H

Measurement setup

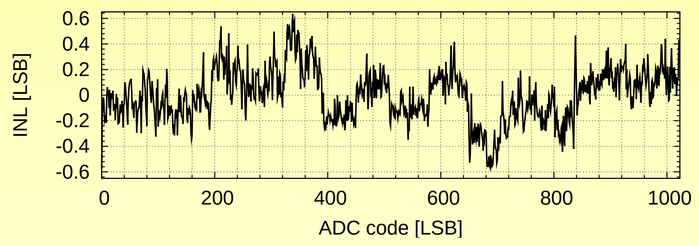


The setup is controlled from a PC computer through GPIB and USB interfaces. The Tektronix AWG2021 is used for input signal and clock generation. Since this 12 bit generator produces single ended signal the conversion to differential is necessary. It is done by a dedicated circuit comprising of fast differential amplifier (THS4505).
The key part of the setup is the FPGA DAQ system built using Altium Nanoboard with Xilinx Spartan-IIE FPGA. Since the data acquisition should be fast the control logic block which reads the data lines from the ADC and stores it in the memory (available on the Nanoboard) is written in the Verilog HDL language. To manage the communication between the NanoBoard and PC the 8051 microcontroller (IP Core) with dedicated firmware is used.
It was verified experimentally that such configuration allows acquiring the data with a sampling frequency up to 100 MHz.

Static measurements results @ 30 MHz



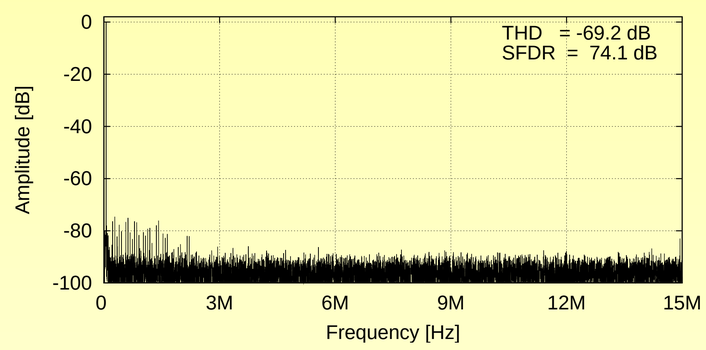
a) Static DNL



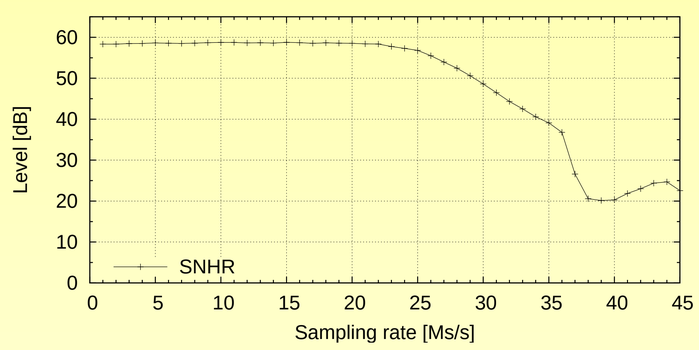
b) Static INL

The static measurements are performed with the input voltage ramped in the range from -1 V to 1 V. To eliminate noise each point is measured several hundred times and then the histogramming method is used for the DNL (figure a) and the INL (figure b) calculations. ENOB computed from the INL curve is equal 9.71.

Dynamic measurements results



a) Sample FFT 40 kHz @ 30 Msps



b) SNHR vs frequency

The dynamic measurements are performed sending a sine signal to the ADC input. A typical FFT spectrum distribution is shown in figure a. The dynamic parameters were studied as a function of sampling frequency and the results of signal to noise ratio (SNHR) are shown in figure b. It is seen that SNHR=58 dB up to about 25 MHz and then starts to decrease. The harmonics parameters are not presented here since it was found that the AWG2021 generates itself harmonics on 40 dB level. In order to check the level of harmonics few measurements were done using the Agilent 33220A arbitrary waveform generator. These measurements showed the harmonics level below 70 dB.

Power

The power consumption was measured at 30 Mhz sampling frequency. For the ADC containing S/H stage the analog and digital currents are 8.6 mA and 6.2 mA respectively. For the version without S/H these currents are 7.1 mA and 5.5 mA respectively. The power may be scaled down at lower sampling frequencies.

Summary

A 10 bits pipeline ADC was designed, produced and found fully functional. Preliminary static measurements show the maximum DNL and INL below 0.43 and 0.64 respectively. The dynamic signal to noise measurements give 58 dB. The performance measurements confirmed the resolution close to 9.5 bits. More detailed dynamic measurements are needed to study better the harmonics. Also the tests of switching ON/OFF functionality need to be performed.

References

[1] H. Abramowicz et al., *Instrumentation of the very forward region of a linear collider detector*, *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 2983-2989, Dec. 2004.

[2] M. Idzik, et al., *The Concept of LumiCal Readout Electronics*, EUDET-Memo-2007-13, http://www.eudet.org/e26/e28/e182/e281/eudet-memo-2007-13.pdf

[3] M. Idzik, K. Swientek, Sz. Kulis, *Development of pipeline ADC for the luminosity detector at ILC*, Proceednings of 15th International Conference on Mixed Design of Integrated Circuits and Systems, MIXDES 2008, 19-21 June 2008, pp. 231–236.

Acknowledgements

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