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A 10-bit 40MS/s pipelined ADC in a 0.13µm CMOS process

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This paper presents a 10-bit analogue to digital converter (ADC) that will be integrated in a general purpose charge readout ASIC that is the new generation of mixed-mode integrated circuits for Time Projection Chamber (TPC) readout. It is based on a pipelined structure with double sampling and was implemented with switched capacitor circuits in eight 1.5-bit stages followed by a 2-bit stage. The power consumption is adjustable with the conversion rate and varies between 15 and 34mW for a 15 to 40MS/s conversion speed. The ADC occupies a silicon area of 0.7mm2 in a 0.13µm CMOS process and operates from a single 1.5V supply.

Summary

In the framework of the research activities at CERN for the EUDET collaboration, a general purpose charge readout chip is being developed. It consists of a programmable charge amplifier and shaper, an analogue-to-digital converter, digital blocks with numerous flexible functions and memory. This paper is focused on the ADC which was entirely developed at CERN and prototyped in a multi project wafer (MPW).

The pipelined ADC architecture was elected since it offers the best compromise in terms of power and area for the speed and resolution required. It was implemented with switched capacitor circuits in eight 1.5-bit stages followed by a 2-bit stage. The half-bit of redundancy in each one of the 1.5-bit stages allows a relaxed accuracy of the comparator's thresholds; therefore low power dynamic comparators were used.

The sampling switches were implemented with complementary low-threshold FETs and guarantee a maximum signal distortion below -72dB over a 20MHz bandwidth. Since low on-resistance is required these switches are relatively large, however a charge injection cancellation scheme with dummy transistors minimizes the amount of change injected. In addition, the bottom sampling technique was employed making the sampling circuit nearly immune to voltage dependant charge injection.

The multiplying digital-to-analogue converter (MDAC) blocks are equipped with rail-to-rail differential output operational amplifiers with 104dB of DC-gain and 314MHz of unitary gain bandwidth. These amplifiers have continuous common mode feedback and a multipart frequency compensation scheme that provides a phase margin of 70º for the main amplifier and 57º for the common mode loop.

The double sampling technique was employed in this design. It consists on the duplication of the sampling circuit permitting a full exploitation of the amplifier's power; therefore the bandwidth is reduced to half of their counterparts in the standard pipelined configuration. A skew insensitive sampling circuit was used to eliminate disparities in sampling time between odd and even samples.

The biasing circuit is based in the beta-multiplier principle that provides constant Gm over a wide range of temperature and is process independent. This circuit allows the tuning of the biasing currents from outside the chip, so the analogue power consumption can match the required sampling speed. In this prototype the power consumption can be tuned from 15 to 34mW for a sampling speed between 15 and 40MS/s.

This design was done in a 0.13µm CMOS process from IBM with analogue options that allowed the use of metal-insulator-metal (MIM) capacitors which are the best available in terms of capacitance accuracy, matching and voltage dependence. This is the same process in which the programmable amplifier shaper amplifier (PASA) was prototyped in a 16-channel chip called PCA16, however with different back end of line (BEOL) options.

For the completeness and enhancement of this ADC a few updates are possible: the inclusion of the redundant sign digit code (RSD) block that combines the data from the stages into a single digital word; the scaling of the MDACs which would lead to a significant reduction of area and power consumption; the integration of a standby mode and the widening of the power efficient operating frequency range.

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