Contribution ID: **91** Type: **Poster**

A self triggered amplifier/digitizer chip for CBM

Thursday, 24 September 2009 16:55 (20 minutes)

The development of front-end electronics for the planned CBM experiment at FAIR/GSI is in full progress. For the charge readout of the various subdetectors a new self triggered amplification and digitalization chip is being designed and tested. The chip will have 32-64 channels each containing a low power/low noise preamplifier/shaper front-end, an 8-9 Bit ADC and a digital post-processing based on a simple FIR-filter. The ADC uses a pipeline architecture based on novel current-mode storage cells. An overview of the architecture and the targeted applications is given and the status of the project is presented.

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Session Classification: POSTERS SESSION

Track Classification: ASIC's