Contribution ID: **59** Type: **Oral**

Front-End Electronics for Pixel Detector of the PANDA MVD.

Tuesday, 22 September 2009 10:10 (25 minutes)

ToPix 2.0 is a prototype in a CMOS 0.13 μm technology of the front-end chip for the hybrid pixel sensors that will equip the Micro-Vertex Detector of the PANDA experiment at GSI.
The Time over Threshold (ToT) approach has been employed to provide a high charge dynamic range (up to 100 fC) with a low power dissipation (15 μW/cell).
In an area of by 100 μm×100 μm each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information. ToPix 2.0 includes 320 pixel readout cells organized in four columns and a simplified version of the end of column readout.

Summary

The PANDA experiment at the future FAIR facility under construction at GSI, Darmstadt, will exploit the antiproton-proton and antiproton-nucleus reactions for precise QCD studies.
The Micro Vertex Detector (MVD) is located in the innermost part of the experimental apparatus and will consist of silicon pixel and silicon strip detectors to obtain precise tracking of all charged particles.
A custom solution for the readout of the pixel detector is motivated by the high track density (up to 12.3 MHz/cm^2) and the absence of a trigger signal.
The front-end ASIC, named ToPiX, will provide the time position of each hit with a resolution of 6 ns rms and a measure of the charge released. The final implementation will consist of a matrix of 100x100 cells with a pixel size 100x100 μm^2, thus covering a 1 cm^2 active area.
A reduced scale prototype, ToPix 2.0, in a CMOS 0.13 μm technology has been designed and tested. The prototype includes two columns of 128 pixel cells, two columns of 32 cells and a simplified version of the end of column readout.
Each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information.
The Time over Threshold (ToT) approach has been employed to provide a charge dynamic range up to 625.000 electrons, corresponding to 2.25 MeV of energy lost in silicon, with a power dissipation of 15 μW/cell from a 1.2 V power supply.
The ToT technique permits to saturate the pre-amplifier but in this way the cross-talk increases. The small discharging feedback current (5 nA) has implication on the uniformity between the different channels. This two issues will be analysed in detail.
The pixel cell input stage is a gain-enhanced cascode amplifier with a feedback capacitor and a constant current discharge circuit. A low frequency differential amplifier in feedback with the input stage allows for leakage current compensation. The output signal time could be up to 18 μs, and this imposes a strong constraint of the low-frequency cut-off.
The input stage is followed by a comparator based on a folded cascode architecture. A configuration register is used to store the DAC values to adjust the comparator threshold voltage and configure the input amplifier to accept the selected signal polarity. The control logic receives the signal from the comparator and stores the value on the time stamp bus at the rising and falling edge in the 12 bit le and te registers.
The pixel matrix is organized into columns. Each column has its separate readout logic made in a fixed priority scheme to read the timestamps of the pixel cells and to read/write the configuration bits. The master clock frequency is 50 MHz.
The test results will be discussed in detail in the presentation and show that the key design goals have been achieved. Ongoing studies to improve further the analog performance will also be addressed.

Primary author: KUGATHASAN, Thanushan (INFN –Sezione di Torino, Università di Torino)

Co-authors: RIVETTI, Angelo (INFN –Sezione di Torino); CALVO, Daniela (INFN –Sezione di Torino); MAZZA, Giovanni (INFN –Sezione di Torino); MIGNONE, Marco (INFN –Sezione di Torino); DE REMIGIS, Paolo (INFN –

Sezione di Torino); WHEADON, Richard (INFN –Sezione di Torino)

Presenter: KUGATHASAN, Thanushan (INFN –Sezione di Torino, Università di Torino)

Session Classification: Parallel session A1 - ASICs

Track Classification: ASIC's