Measurement of the performances of a Low-Power Multi-Dynamics Front-End for Neutrino Underwater Telescope Optical Modules

D. Lo Presti[a], L. Caponetto[b], G.V. Russo[a], N. Randazzo[c], V. Sipala[a] , E. Leonora[c]
On behalf of the NEMO collaboration

a University of Catania, Department of Physics and Astronomy, Catania, Italy
b INFN Catania/CNRS-IN2P3-CPPM, Marseille, France
c Istituto Nazionale di Fisica Nucleare, Sezione di Catania, Italy

domenico.lopresti@ct.infn.it

Abstract

A solution for a system to capture signals in the Optical Module of an underwater neutrino telescope[1,6] is described, with focus on power consumption and signal dynamics considerations. All the design specification derive from considerations regarding the signals and their acquisition and are made starting from the most general hypothesis possible, so that they will be valid for any underwater Cherenkov neutrino telescope.

I. Introduction

A front-end board, the FE-ADC [3], using a consumer ADC, has been designed and realized. It is aimed at the demonstration of the advantages of the proposed architecture fitting the specifications of power dissipation, multi-input dynamics and signal reconstruction has been realized.

The performances of this board have been accurately measured, both stand alone and coupled to the PMT foreseen by the NEMO collaboration, and are presented and discussed.

The results meet the requirements and establish the basis for the design of the definitive front-end architecture employing the SAS (Smart Analogue Sampler) chip [4] in place of an ADC.

II. Description of the FE-ADC

In order to validate the proposed architecture, a front-end board has been designed. The block diagram of the board is shown in figure 1. All the functionalities foreseen for the final front-end board has been implemented. The sampling and A/D conversion of the PMT interface output signal are performed by a consumer 200 MHz 12 bit ADC, the AD9230 by Analog Device. The ADC output data are stored in a FIFO inside the FPGA only when a validation signal, the SOT (Signal Over Threshold) is high, corrisponding to the OutA crossing a suitable threshold. In this way it is possible to perform zero suppression and minimize dead time. The data transmission mechanism is the same developed, and full working, in the Front-end board used in NEMO Phase-1 [2].

If a signal exceeds the 512 pe it is possible to sample the integrator output of the PMT interface.

The sampling frequency is again 200 MHz but the stored data are taken every 10 samples. In this way using the same ADC it is possible to have samples of the integrator at 20 MHz.

The FIFO in the FPGA has a depth of 1 Ksample. This allows an instantaneous event rate up to 1 MHz without dead time, for signal in the range 1 ÷ 512 pe and time width below 100 ns.

When the integrator signal is used, the maximum record length in time is 50 μs.

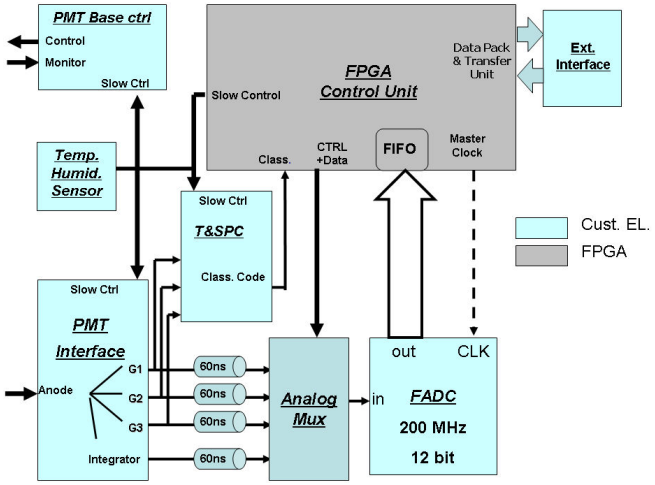

Figure 1 Block diagram of the FE-ADC board

The AD9230 has only one input channel and this input is connected, according to signal classification, to the correct PMT interface output through a fast analog multiplexer. This multiplexer is controlled by the Control Unit implemented in the FPGA.

The multiplexer changes its output according to the signal classification continuously, so, for example, if a signal crosses the over range threshold of the first input dynamics, the ADC will always sample the signal in the correct dynamics.

The samples of a signal together with the cardinal sine interpolation are shown in figure 2.

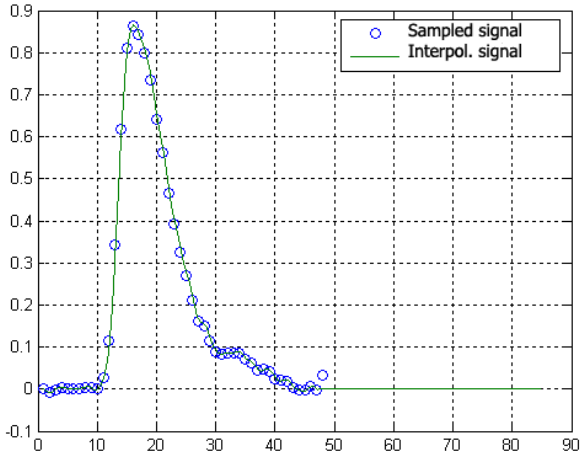

Figure 2: An example of waveform reconstructed using cardinal sine interpolation.

In this way, knowing the classification corresponding to each sample and the PMT interface gain calibration, it is possible to reconstruct the input signal Off-Line. An input linear range of 512 pe and an overall input dynamics, using the integrator output, up to 10000 pe are achieved.

III. TEST RESULTS

The PMT signal has been acquired and used as a parametric input waveform.

The FE-ADC board has been tested using an arbitrary waveform generator for the PMT emulated input signal generation. A picture of the FE-ADC board is shown in figure 3.

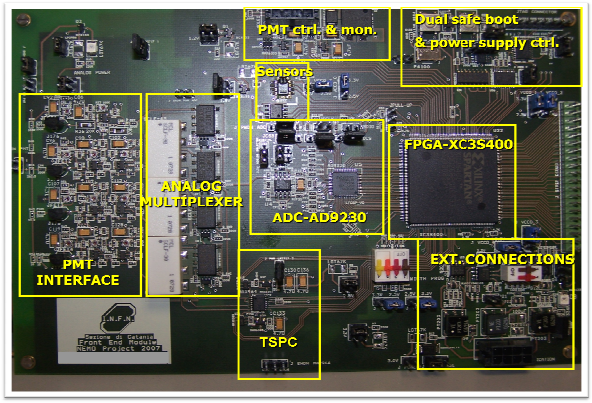

Figure 3 A picture of the FE-ADC board

In the following, the results of the measurement of the PMT coupled to the FE-ADC board as the front-end electronics are presented. A data acquisition firmware has been designed for this purpose.

A. *Charge resolution*

The charge of an acquired signal is calculated off-line integrating the interpolated waveform of the signal itself.

In this way, it is possible to draw the charge spectrum and evaluate the gain and the resolution of the system, PMT an FE-ADC.

On the basis of the measurements, the gain of the PMT can be reduced to $1{,}36 \cdot 10^7$, by a factor of about 3,6, without affecting the optimal signal to noise ratio. This is a great advantage from the point of view of the ageing allowing, furthermore, an increase of the PMT output linear range from 100 to about 1000 photo-electrons.

In figure 4, the single photo-electron charge spectrum of the system at the optimal gain is shown.

The peak to valley and the resolution of the PMT, as measured stand alone with standard setup in single photo-electron conditions, remain unchanged, respectively 2 and 20%.

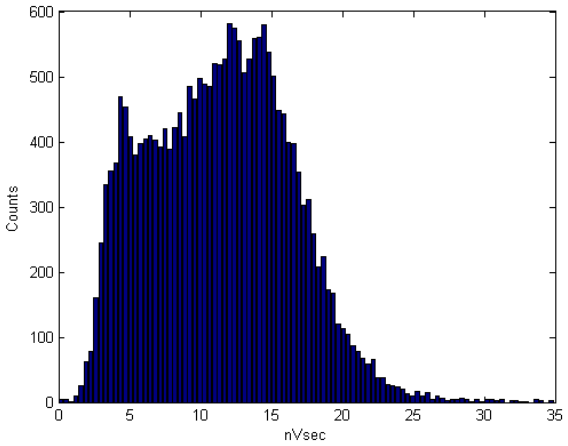

Figure 4: The single photo-electron charge spectrum measured using the FE-ADC

B. *Time resolution*

The time stamp of an incoming signal consists of two terms: rough and fine time stamps.

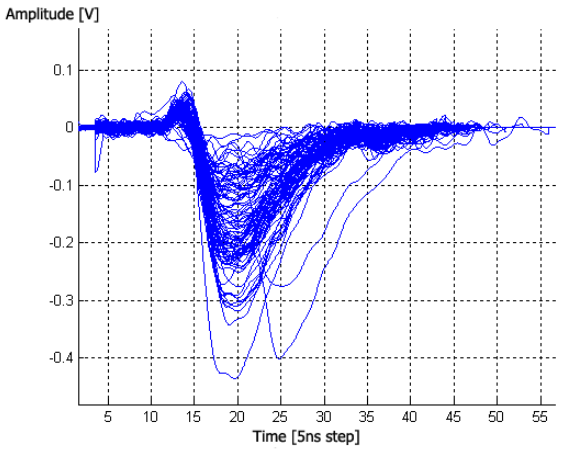

Figure 5: An example of the CFD software output

The rough time stamp mechanism consists of a 10 bit 200 MHz counter implemented in the FPGA. The 200 MHz clock is derived by the 20 MHz Master Clock by means of a DCM inside the FPGA. The measured jitter is below 300 ps. The clock is a LVDS signal and drives the ADC. In the final front-end, the SAS chip will use the same clock.

The fine time stamp is calculated by a costant fraction discriminator (CFD) software applied to the interpolated waveform. An example of the sotware output is shown in figure 5.

Using a laser source at a repetition frequency of 10 kHz and the time stamp of the signals acquired by the system it was possible to measure the time resolution of the whole system. The resolution has different components: the laser pulses jitter, the PMT time resolution, the front-end time stamp reconstruction resolution. The measured overall time resolution is of about 1,4 ns. The laser pulse jitter is negligible and the PMT resolution, measured using standard setup is of about 1,25 ns. In figure 6, the time stamp spectrum is shown.

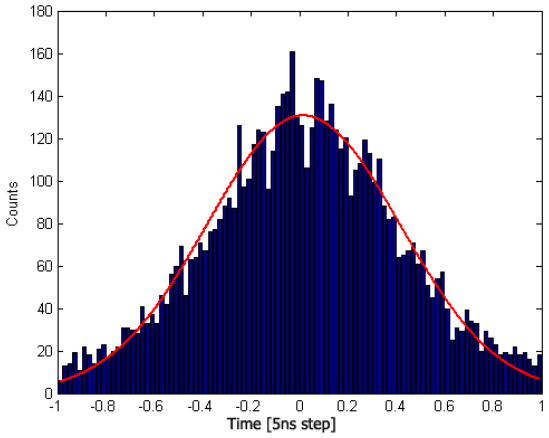

Figure 6: The time stamp spectrum for the system in single photo-electron conditions

C. *Double hit resolution*

In order to measure the double hit resolution, which is a crucial parameter for our application, a dedicated setup has been developed. Using a splitter for optical fiber to obtain two optical path with different time delay it is possible to produce starting from a signal a double hit with the desired time separation. A measurement of the reconstruction performances varying the time separation has been performed. An example of the double hit waveform acquired is shown in figure 7.

The signal filtering and the sampling frequency have been optimized to obtain a double hit resolution of 20ns.

D. *Control Unit*

The Control Unit has been implemented in the FPGA, a Spartan3 by XILINX and manage all the operations in the FE-ADC board: the PMT supply voltage control and supervision, the thresholds of the classification, the ADC samples storage, filtering and transmission, the communication and the on board sensors.

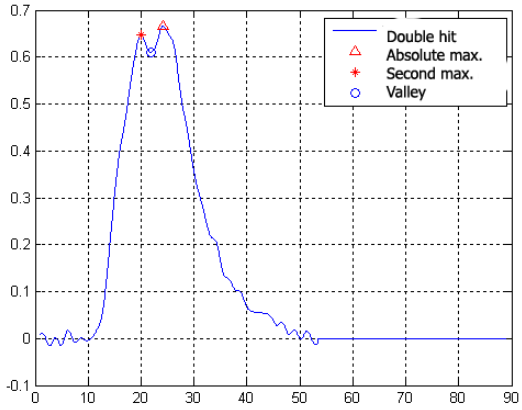

Figure 7: A typical double hit waveform with 20 ns time separation

E. *Overall performances*

The emulation board has been fully tested in its overall performances and the technological and architectural choices are fully compliant with the mechanical and experimental specifications.

The main performances of the FE-ADC board coupled to the PMT are summarised in Table 1.

Table 1: main performances of the FE-ADC board coupled to the PMT

Multi-dynamics: • 3 linear dynamic range up to 512 pe • charge dynamic range up to 10000 pe • signal classification
Negligible dead time (@ 300 KHz BG in 10” PMT)
5 ns time stamp online
600ps time stamp offline
20ns double hit resolution
PMT low gain = $1{,}36 \cdot 10^7$ • high linear range • lower dark current • longer PMT operating life

The main feature of the FE-ADC are summarised in Table 2.

Table 2: Main feature of the FE-ADC board.

FE-ADC inside or outside the Optical Module
Power supply (analog and digital) - 290 mA @ 5 V (187 mA ADC) 1,4 W (70% yield)
Dual Safe Boot - FPGA back-up firmware
PMT control (ISEG base interface)
ADC 200 Msps 12 bit
200 MHz lvds sampling clock generation (DCM)
Time stamp and classification (settable by slow control)
Temperature and humidity Sensors
Istantaneous rate monitor

The total power dissipation is about 1,5 W measured with a 5 V power supply. Considering that the ADC counts for the 64% of the power consumption and that the foreseen power consumption of the SAS chip is 60 mW, the definitive front-end board will have a power consumption of about 700 mW.

IV. CONCLUSIONS

The development of the emulation board demonstrates the advantages of the proposed architecture fitting the specifications of power dissipation, multi input dynamics, signal reconstruction establishes the basis for the definitive design of the final front end board using the SAS chip. As soon as the chip will be available, the whole front-end have been tested together with the PMT.

The results of the measurements show that all the specifications for the Optical Module front electronics have been satisfied. The use of the final version of the SAS chip will allow for the total power consumption to be further reduced.

V. REFERENCES

[1] Nemo website, nemoweb.lns.infn.it

[2] F.Ameli, M.Bonori, C.A.Nicolau, A 200 MHz FPGA-based PMT Acquisition electronics for Nemo experiment. Proceeding of VLVnT Workshop,231-234,Nikhef, Amsterdam 2003, http://www.vlvnt.nl

[3] D. Lo Presti, G. V. Russo, L. Caponetto,N. Randazzo, et al., A VLSI Full Custom ASIC Front End for the Optical Module of the NEMO Underwater Neutrino Detector, IEEE Transactions on Nuclear Science, Vol. 53, No. 3 (June, 2006) issue.

[4] L. Caponetto, D. Lo Presti, G.V. Russo, N. Randazzo et al., Design study of a low power, low noise front-end for multianode silicon drift detectors., Nuclear Instruments and Methods in Physics Research A, v. 552, iss. 3, pp. 489-512, 2005

[6] E. Migneco et al., Status of NEMO, Proc. Second Int. Workshop on large neutrino telescopes, Nucl. Instr. Meth. A567 (2006) 444