Contribution ID: **58** Type: **Poster**

Measurement of the performances of a Low-Power Multi-Dynamics Front-End for Neutrino Underwater Telescope Optical Modules

Thursday 24 September 2009 16:55 (20 minutes)

A proposal for a system to capture signals in the Optical Module of an underwater neutrino telescope is described, with focus on power consumption and dynamics considerations. All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any underwater Cherenkov neutrino telescope.
A front-end board, the FE-ADC, using a commercial ADC, has been designed and realized. It is aimed at the demonstration of the advantages of the proposed architecture fitting the specifications of power dissipation, multi input dynamics and signal reconstruction has been realized.
The performances of this board have been accurately measured, both stand alone and coupled to the PMT foreseen by the NEMO collaboration, and are presented and discussed.
The results meet the requirements and establish the basis for the definitive design of the final front-end architecture employing the SAS (Smart Analogue Sampler) chip.

Summary

In order to validate the proposed architecture, a front-end board has been designed. All the functionalities foreseen for the final front-end board have been implemented. The sampling and A/D conversion of the PMT interface output signal are performed by a commercial 200 MHz 12 bit ADC. The ADC output data are stored in a FIFO inside a FPGA only when a suitable validation signal occurs. In this way it is possible to perform zero suppression and minimize dead time. Together with the data, the classification and the 200MHz time stamp must be transferred. The data transmission mechanism is the same developed, and full working, in the front-end board used in NEMO Phase1 [1].
This FE-ADC board test is thought in order to measure the overall performances and to verify that the technological and architectural choices are fully compliant with the mechanical and experimental specifications.
The total power dissipation is about 1 W measured with a 5 V power supply.
All the results are extremely important for the design of the front board containing the SAS chip. Actually all the architectural solution foreseen for the SAS front-end board have been implemented in the front end board.
The SAS chip will be sent to foundry for production in March 2009. The SAS chip will allow for a further power dissipation reduction of a factor 3.

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Session Classification: POSTERS SESSION

Track Classification: Production, testing and reliability