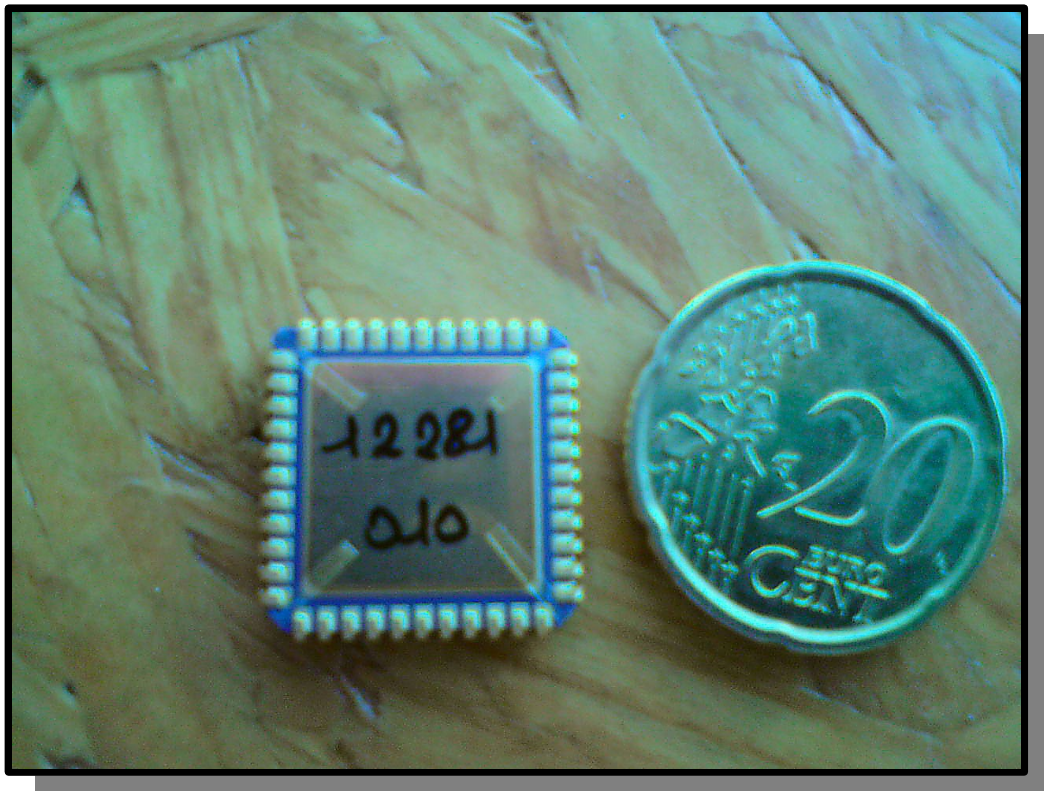
SAS: Smart Analogue Sampler for the Optical Module of a Cherenkov Neutrino Detector



L.Caponetto for the KM3NeT Consortium

TWEPP'09 - Paris
24 Sep 2009

The KM3Net Consortium

41 Institutes from 10 European Countries + participants from the three present-day Mediterranean ν projects (ANTARES, NEMO, NESTOR)

Cyprus:	Univ. Cyprus Nicosia
France:	CEA/Saclay, CNRS/IN2P3 (APC Paris, CPPM Marseille, IReS Strasbourg), Univ. Haute Alsace/GRPHE), IFREMER
Germany:	Univ. Erlangen, FTZ (Univ. Kiel), Univ. Tübingen
Greece:	HCMR Anavissos, HOU Patras, NCSR Athens, NOA/Nestor Athens, Univ. Athens
Ireland:	DIAS Dublin
Italy:	CNR/ISMAR, INFN (Univs. Bari, Bologna, Catania, Genova, Napoli, Pisa, Roma-1, LNS Catania, LNF Frascati), INGV, Tecnomare SpA
Netherlands:	NIKHEF/FOM Amsterdam, Univ. Amsterdam, Univ. Utrecht, KVI (Univ. Groningen), NIOZ
Romania:	ISS Bucharest
Spain:	IFIC (CSIC) Valencia, Univ. Valencia, UP Valencia
UK:	Oceanlab (Univ. Aberdeen), Univ. Leeds, Univ. Liverpool, Univ. Sheffield

Particle/Astroparticle institutes (33) – Sea science/technology institutes (8) – Coordination

L.Caponetto caponetto@cppm.in2p3.fr

Background: water Cherenkov detectors

- Neutrino telescopes: based on the detection of the secondary particles produced in neutrino interactions
- Small interaction cross section of neutrinos allows them to come undisturbed from far astrophysical objects: large target mass is required for the detector
- Detection principle:
  - A matrix of light detectors (PMTs) deeply immersed in a transparent media
    - Large target volume for neutrino interactions
    - Shielding against secondary particles
    - Transmission of Cherenkov photons
  - Accurate reconstruction of the trajectory of the secondary particles requires:
    - PMT + electronics resolution better than 2 ns
    - Positioning precision better than 40 cm

Also see talks given by G. Hallewell (parallel session B1) "Deep-sea data transfer at the KM3NeT neutrino telescope" and by M. Sedita (parallel session B4 "KM3NeT Power and Submarine Cable Systems for the kilometer cube Neutrino Telescope")

Readout system

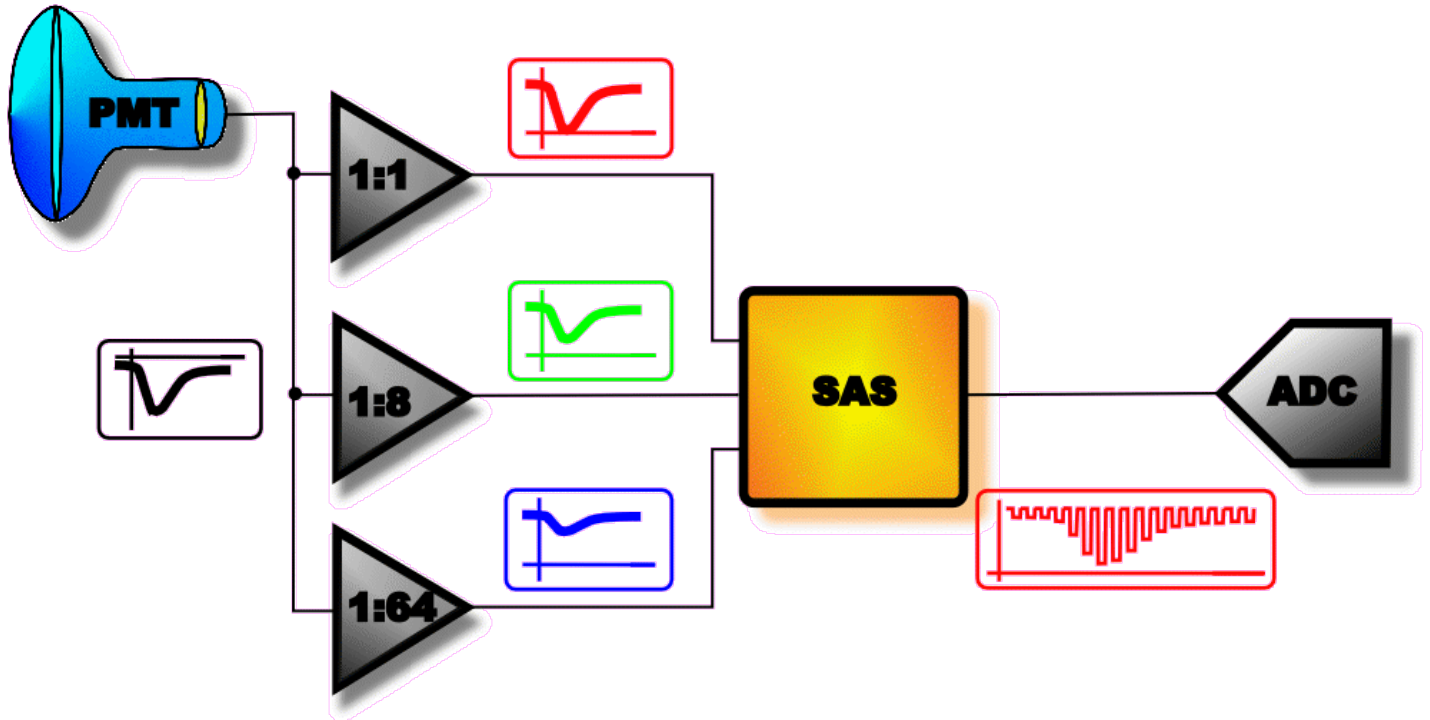
- Signal baseline: 75-80 kHz range (Catania "Test-site" ^{40}K decay: varies with PMT area and seawater)
- Rate distribution shows bursts extending to several hundreds kHz
- Rare neutrino signals embedded in random background: discrimination obtained offline
  - Trigger based on time/position correlations produced by the traversing particle
- Single photoelectron hits above a threshold are time stamped
  - Time and charge of the detected light signals (hits) are relevant information
  - "Oscilloscope-mode" acquisition
- Goal: storing and forwarding of digitized pulse waveforms up to a rate of about 300kHz

Front-end electronics considerations

- Single photoelectron (spe) hits are short pulses with typical FWHM ~10 ns (without filtering and with a PMT gain of 5×10^7)
- spe hits on a 50 Ohm anodic load have ~3 ns rise time and ~50 mV amplitude with spectrum above 100 MHz
- PMT signal amplitude linearly grows with light intensity up to 100 photoelectrons
  - Higher anodic loads allow larger signal amplitude and dynamic
- Proposed shaping and filtering of PMT signal:
  - 70 dB reduction of frequency components above 100 MHz
  - spe hits become short pulses not larger than 100 ns
  - The shaped rise time of the pulses is ~15 ns
    - (interpolated) time and charge reconstruction of 200 MS/s sampled hits shows 200-300ps time resolution and max 3 % charge reconstruction error
- A prototype board with ADC sampling at 200 MHz has been realized:

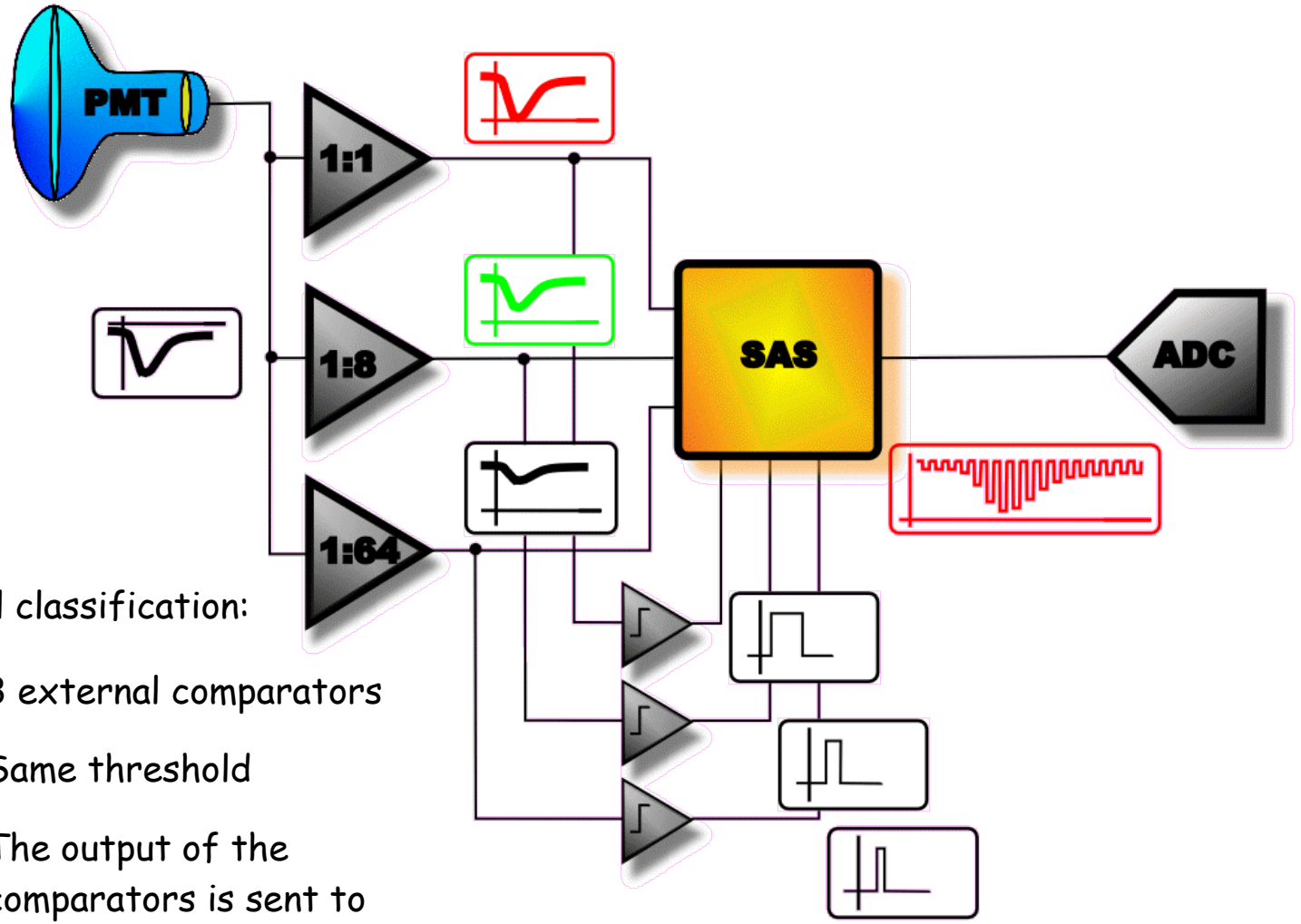
  See poster presented by V. Sipala "Measurement of the performances of a Low-Power Multi-Dynamics Front-End for Neutrino Underwater Telescope Optical Modules"

Block diagram of the proposed front-end architecture



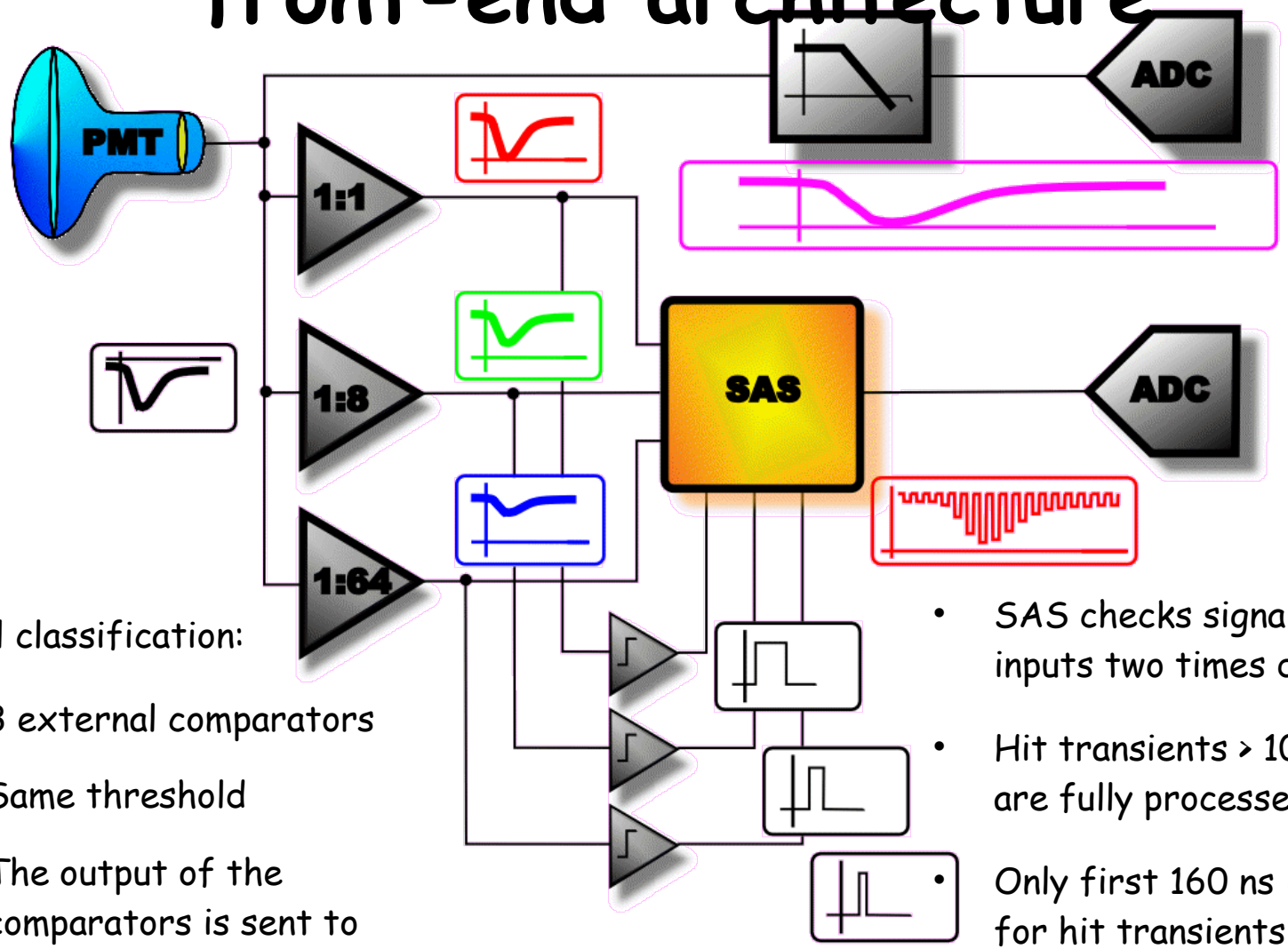
- The same PMT anode signal is filtered, level shifted and attenuated with three different gains
  - 200 MS/s SAS acquisition is started by an external trigger based on threshold crossing
  - The three replica signals are all sampled by the SAS for a minimum time window of 160 ns
  - Only stored analogue samples of one signal channel are sent to the ADC for the conversion
    - Signal classification uses hardware external to the SAS

Block diagram of the proposed front-end architecture



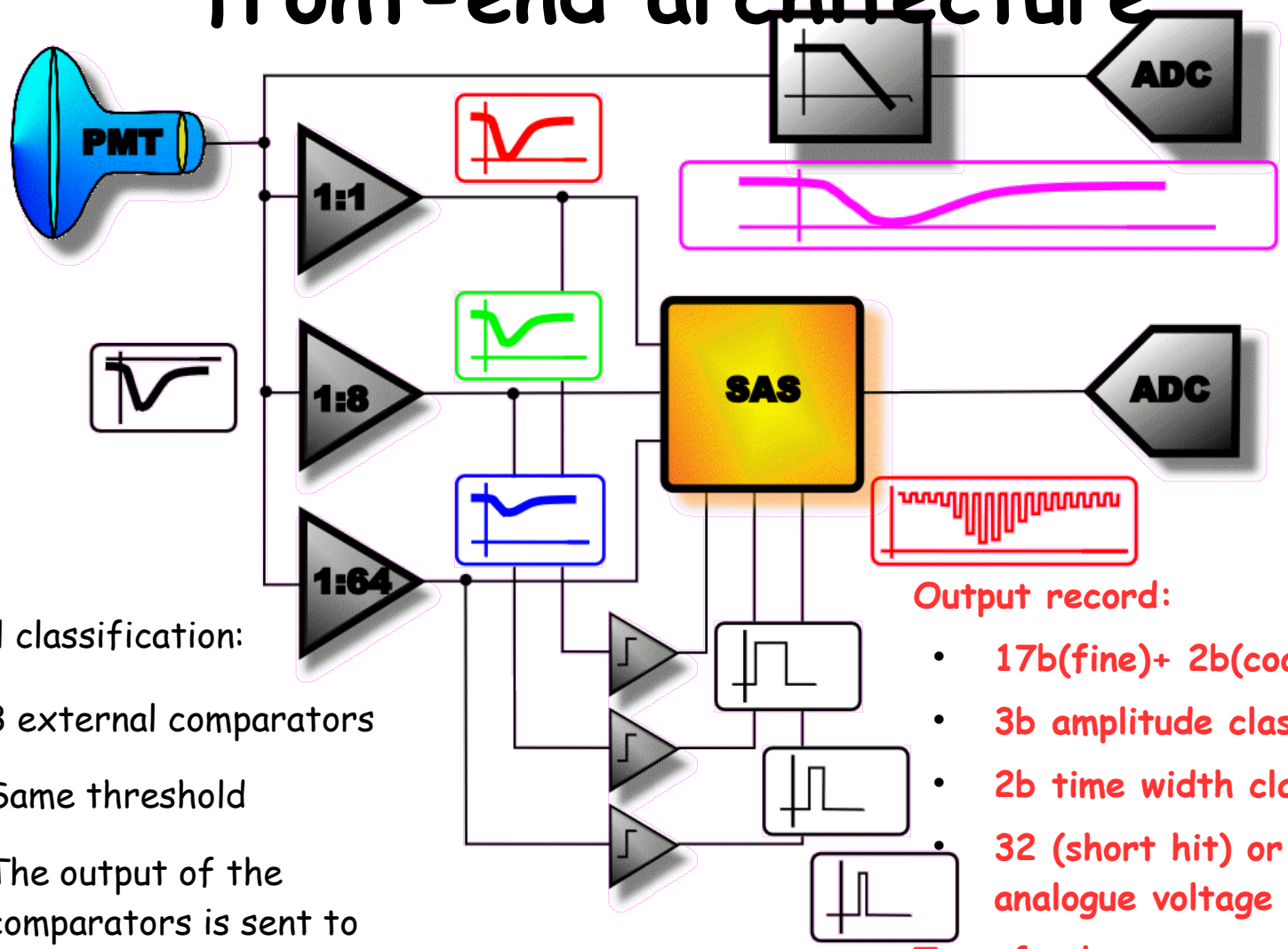
- Signal classification:
  - 3 external comparators
  - Same threshold
  - The output of the comparators is sent to the SAS

Block diagram of the proposed front-end architecture



- Signal classification:
  - 3 external comparators
  - Same threshold
  - The output of the comparators is sent to the SAS
- SAS checks signal classification inputs two times during acquisition
- Hit transients > 100 ns and < 790 ns are fully processed by the SAS
- Only first 160 ns information used for hit transients > 790 ns
  - External integration path

Block diagram of the proposed front-end architecture



- Signal classification:
  - 3 external comparators
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  - The output of the comparators is sent to the SAS

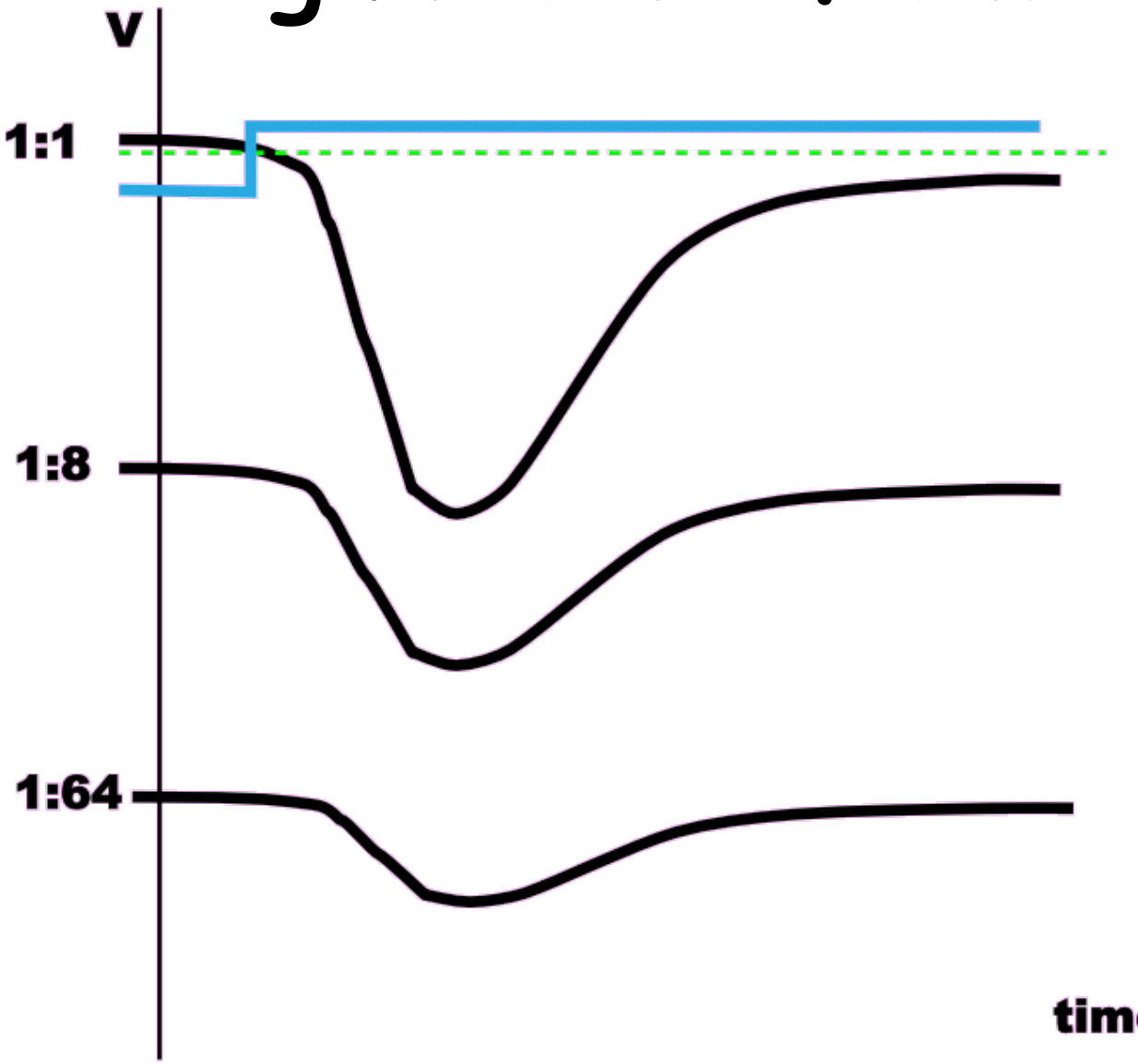
Output record:

- 17b(fine)+ 2b(coarse) timestamp
- 3b amplitude classification
- 2b time width classification
- 32 (short hit) or 32+3x128 analogue voltage samples

Transfer latency:

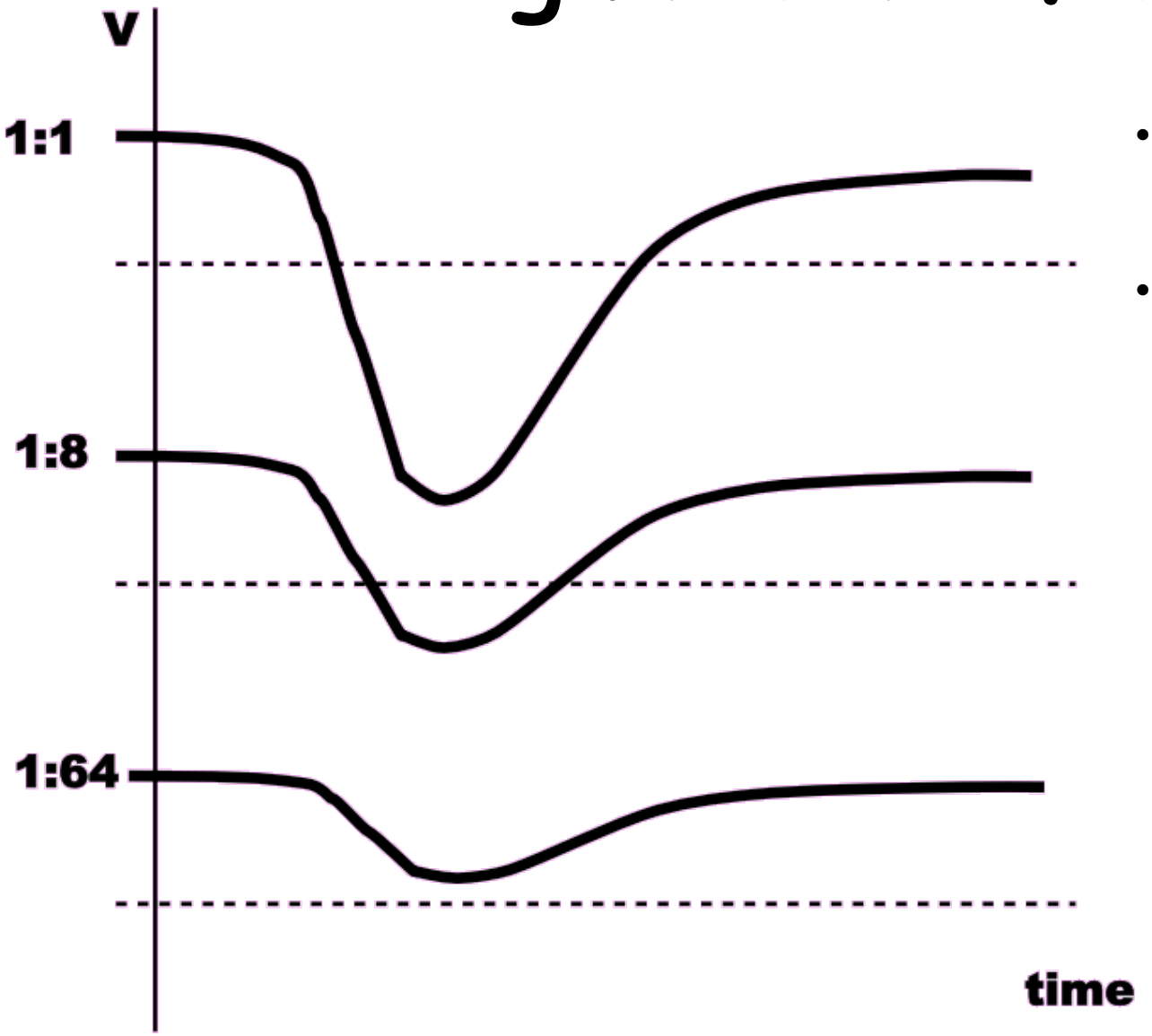
- 1.6us(min) or 20.8us(max)

Signal classification: example



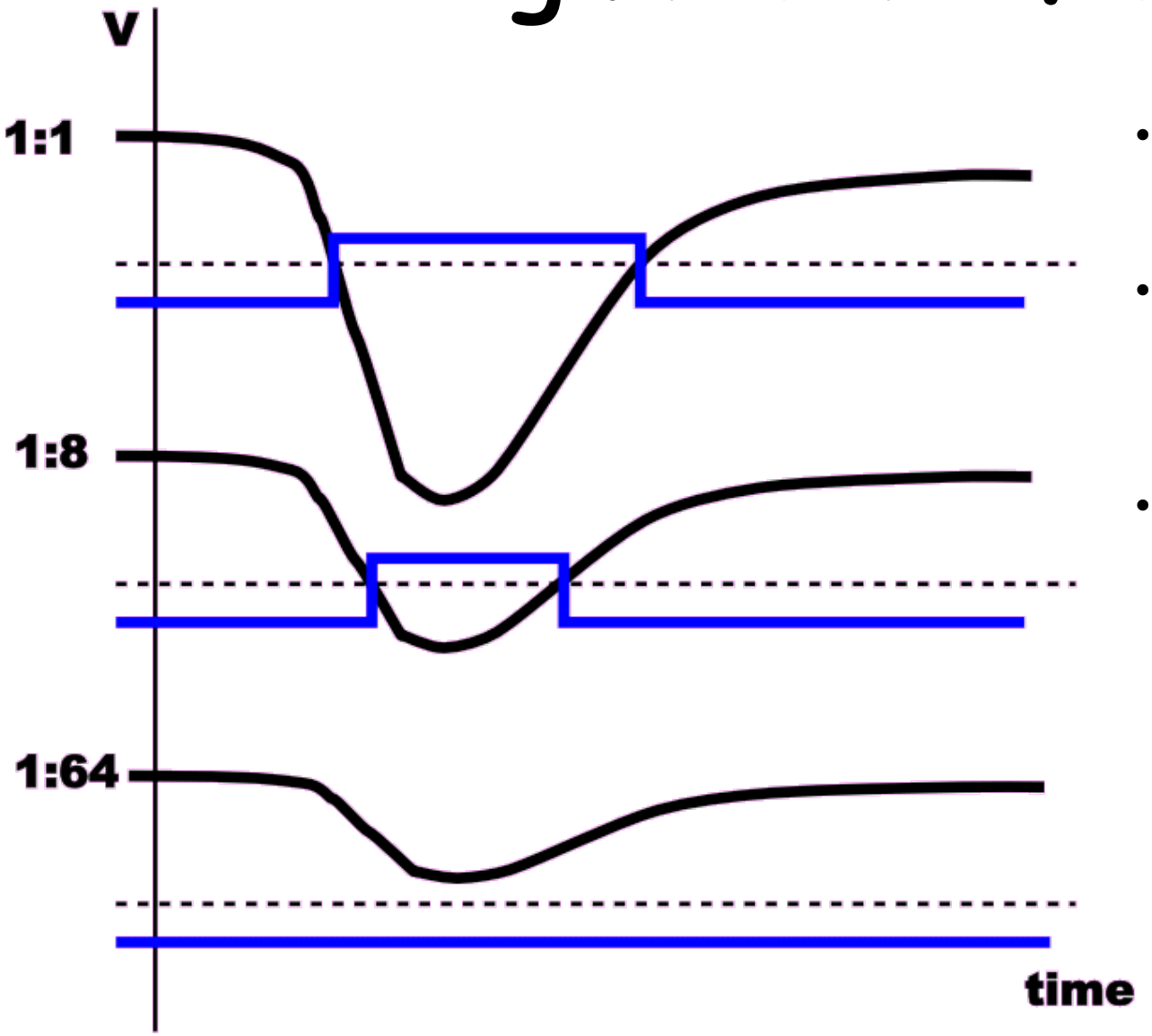
- 1:1 replica is confronted with a first threshold

Signal classification



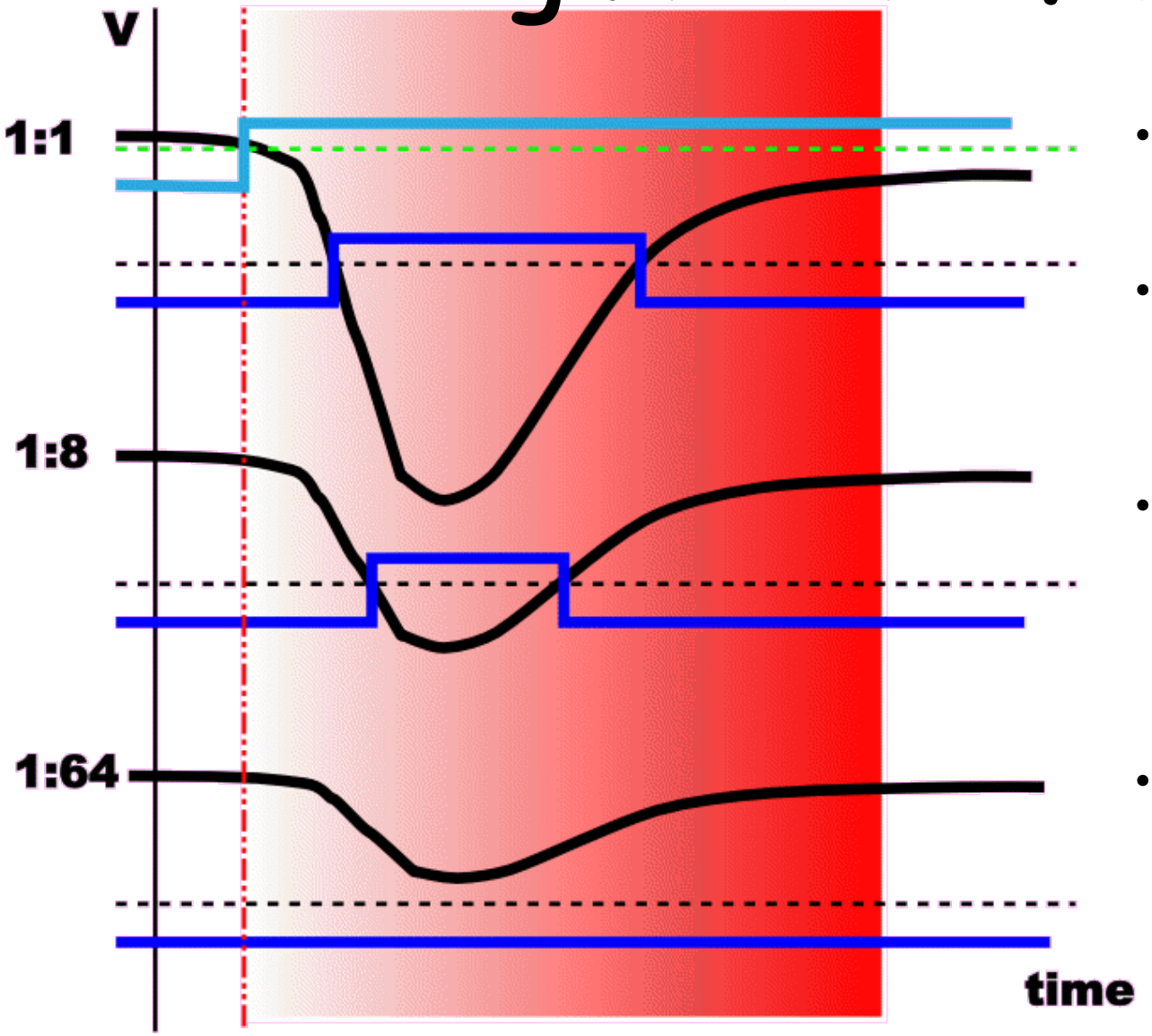
- 1:1 replica is confronted with a first threshold
- At same time all three signals are confronted with a second threshold

Signal classification



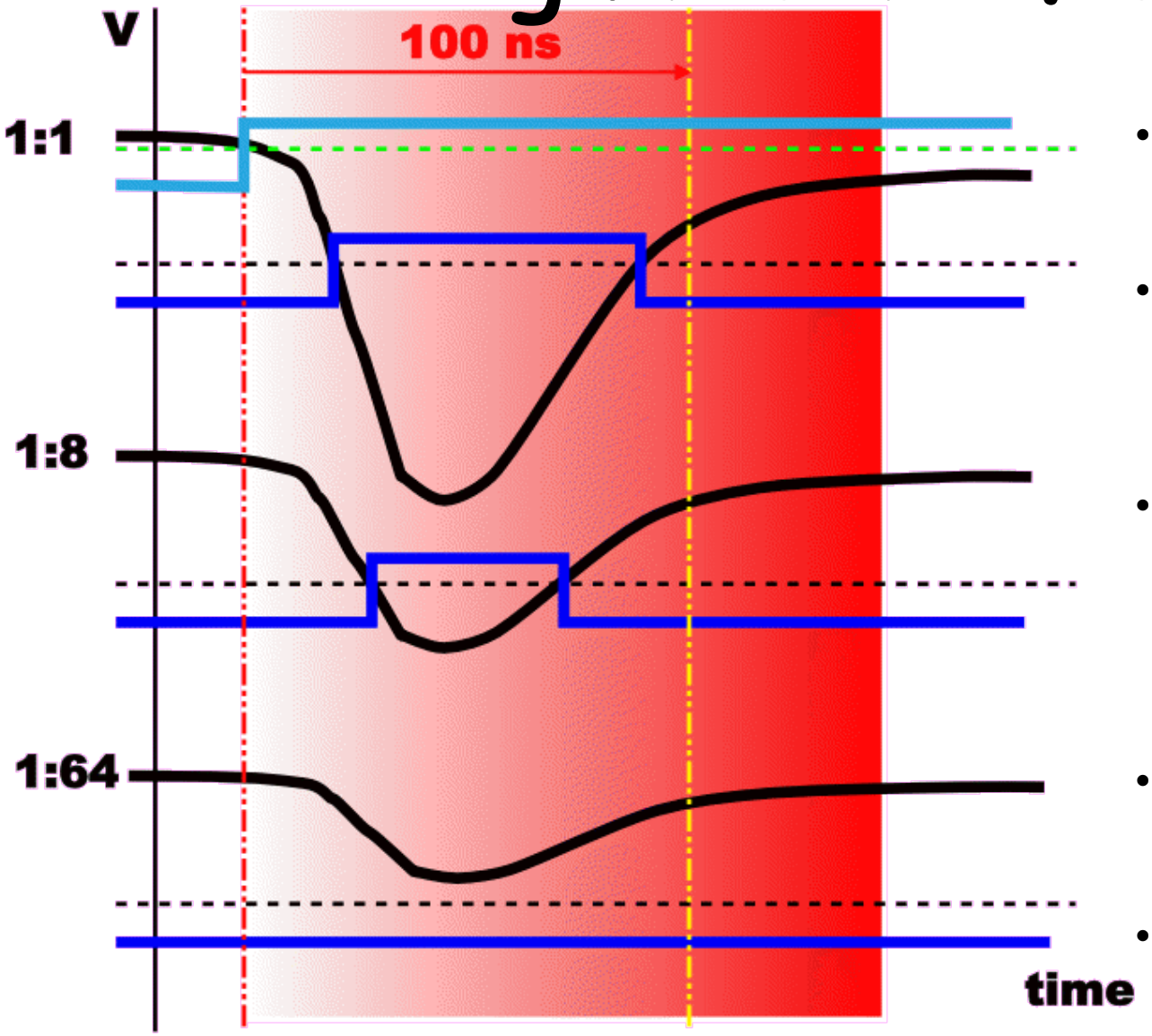
- 1:1 replica is confronted with a first threshold
- At same time all three signals are confronted with a second threshold
- The output of all the comparators is read by the SAS for signal classification

Signal classification



- 1:1 replica is confronted with a first threshold
- At same time all three signals are confronted with another threshold
- The output of all the comparators is read by the SAS for signal classification
- The acquisition time is fixed (160 ns)

Signal classification

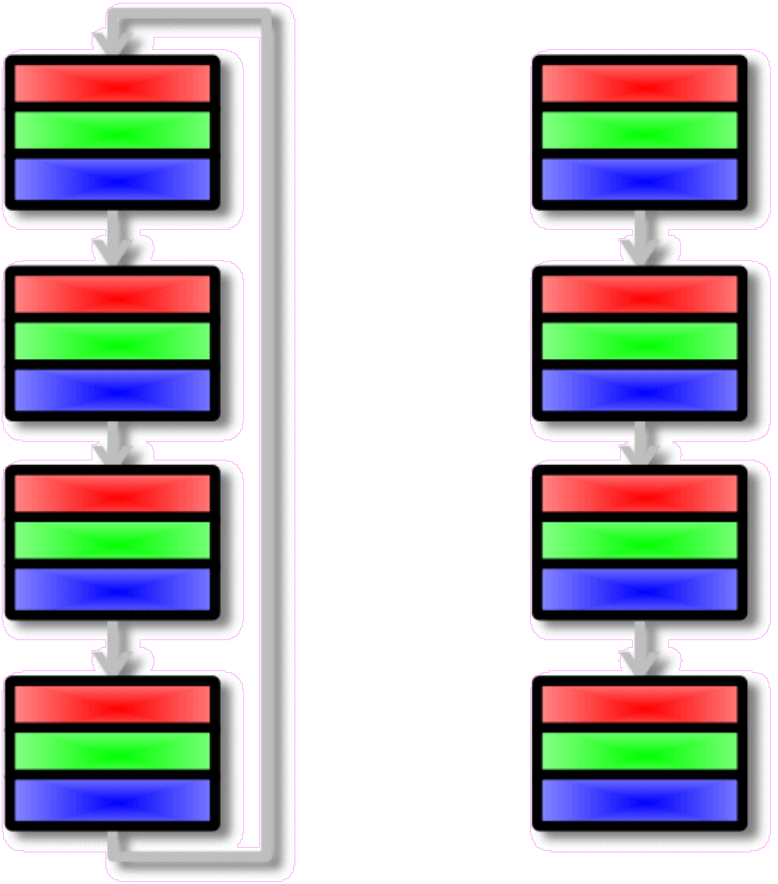


- 1:1 replica is confronted with a first threshold
- At same time all three signals are confronted with another threshold
- The output of all the comparators is read by the SAS for signal classification
- The acquisition time is fixed (160 ns)
- First classification made after 100 ns from trigger

Proposed architecture: summary

- FIFO structure of 4 short analogue memories
  - Oscilloscope mode recording and time stamping of hits <160 ns
  - Target is 300 kHz sustainable rate of short pulses
- Single (long) analogue memory to sample and store transients hits longer than 160 ns
  - 640 ns + 160 ns maximum storing length
- 4 acquisition channels:
  - 3 replicas (different attenuation) of the PMT anode signal
    - Hit arrival information could be reconstructed from the most adapt channel
    - Replica channels not exploiting the full dynamic will be not converted
  - External low pass filter + dedicated ADC
    - Provides information from hits longer than 640 ns + 160 ns
- Dedicated classifier circuitry for PMT signals

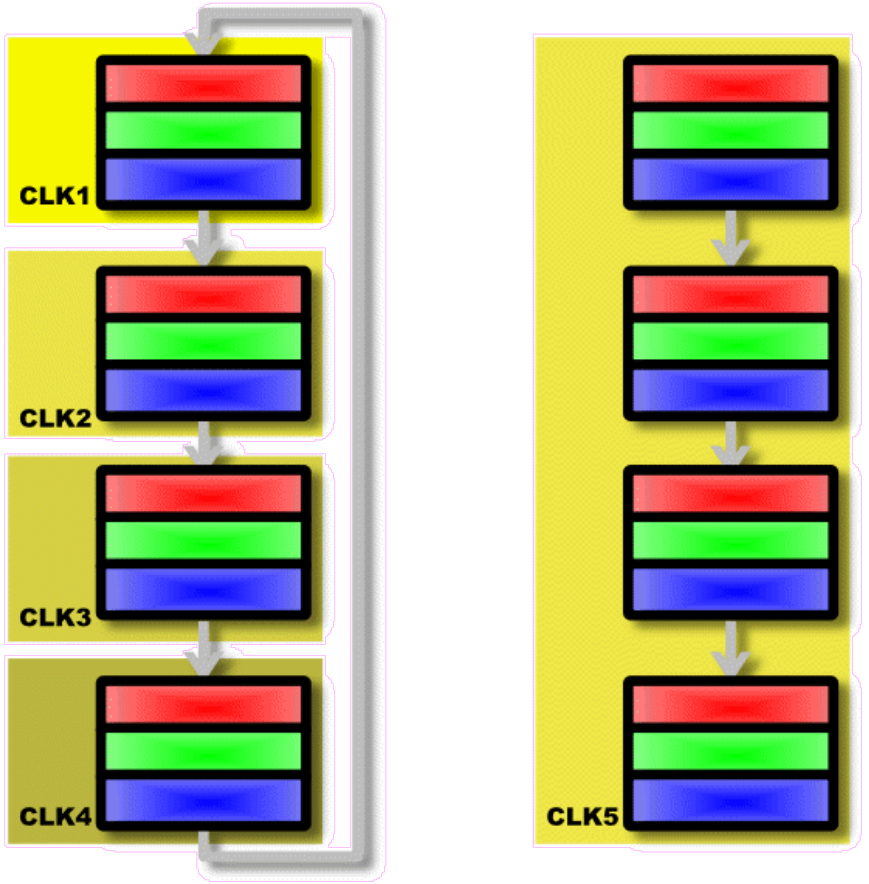
ASIC architecture



Analogue memories building blocks

- Same macrocell is replicated x8
- Each macrocell contains:
  - 3 x 32 analogue sampling cells
  - Write/read addressing units

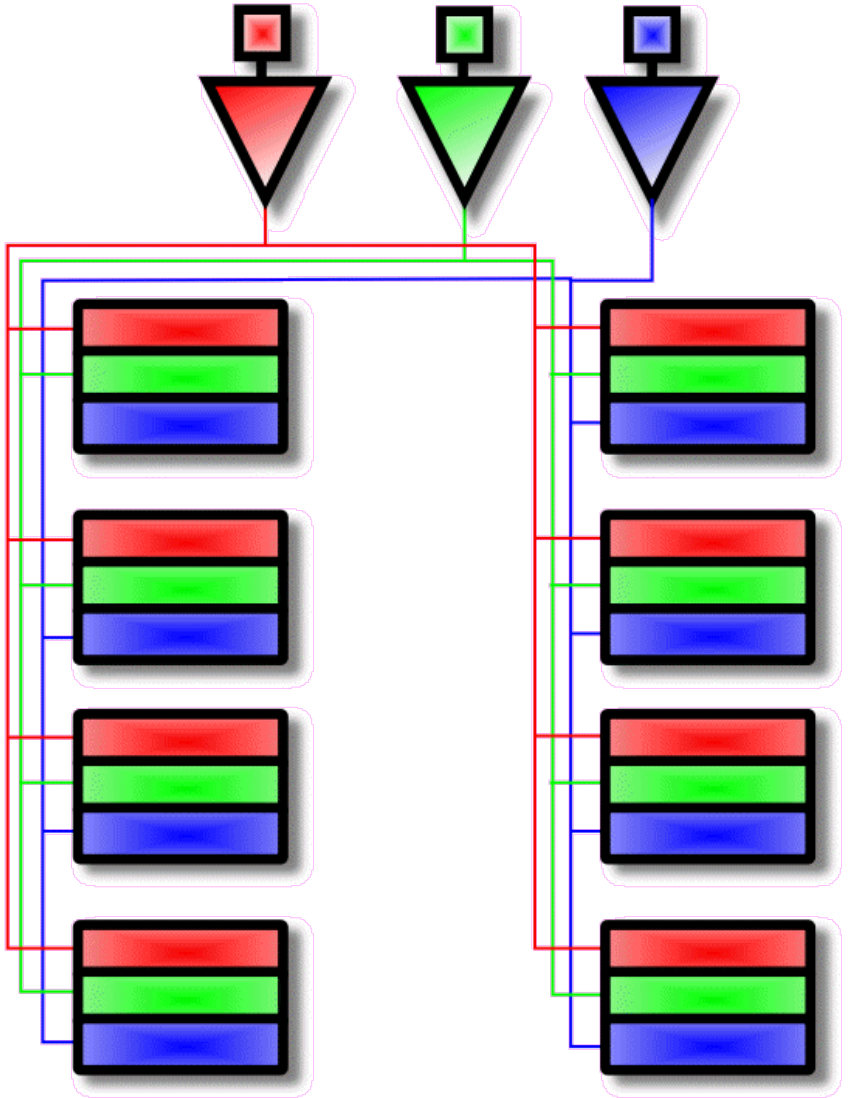
ASIC architecture



Analogue memories building blocks

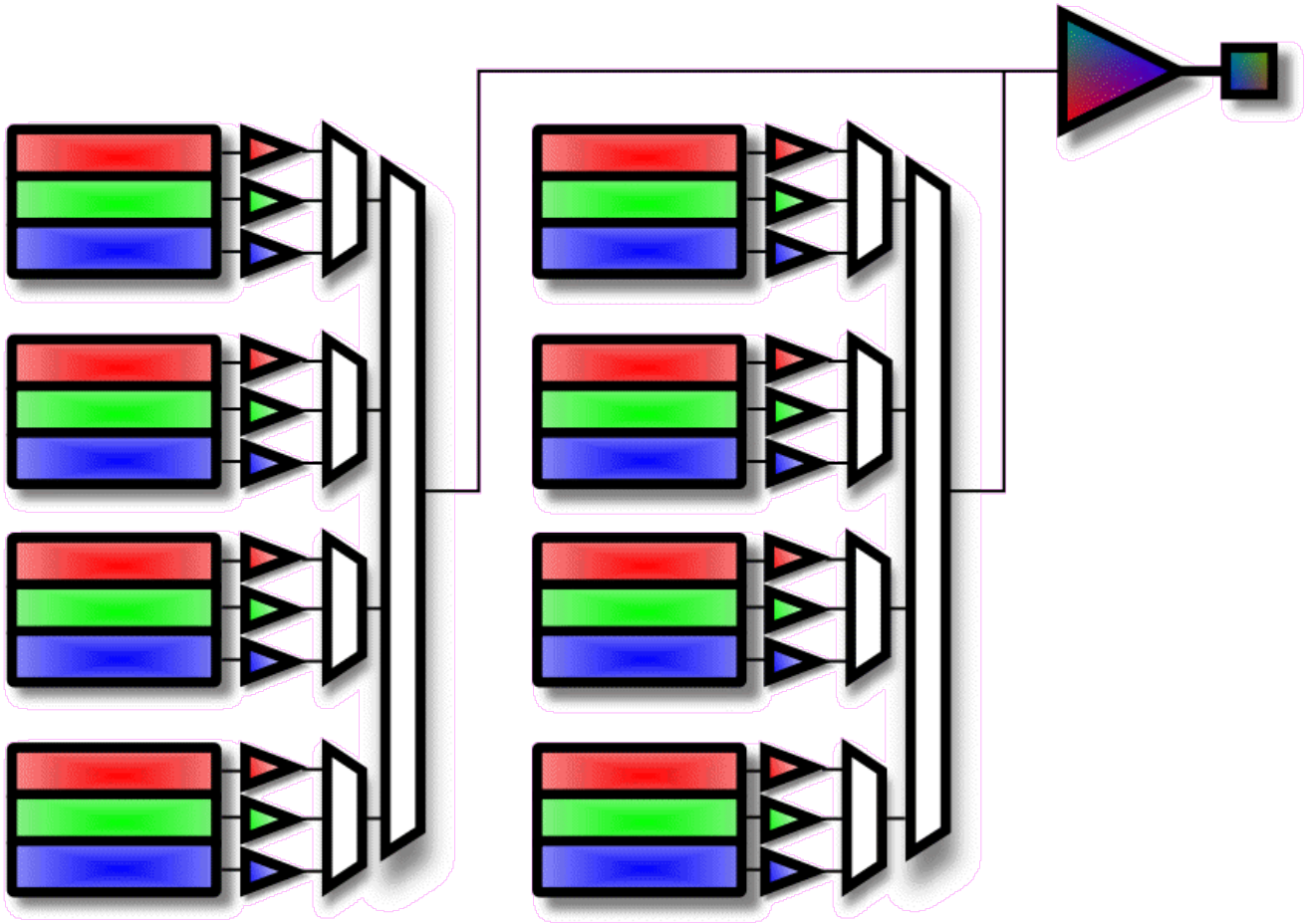
- Same macrocell is replicated x8
- Each macrocell contains:
  - 3 x 32 analogue sampling cells
  - Write/read addressing units
- 5 different clock domains
  - 5 independent sampling units
  - 4 connected as circular FIFO
  - 5th unit stores long transient

ASIC architecture



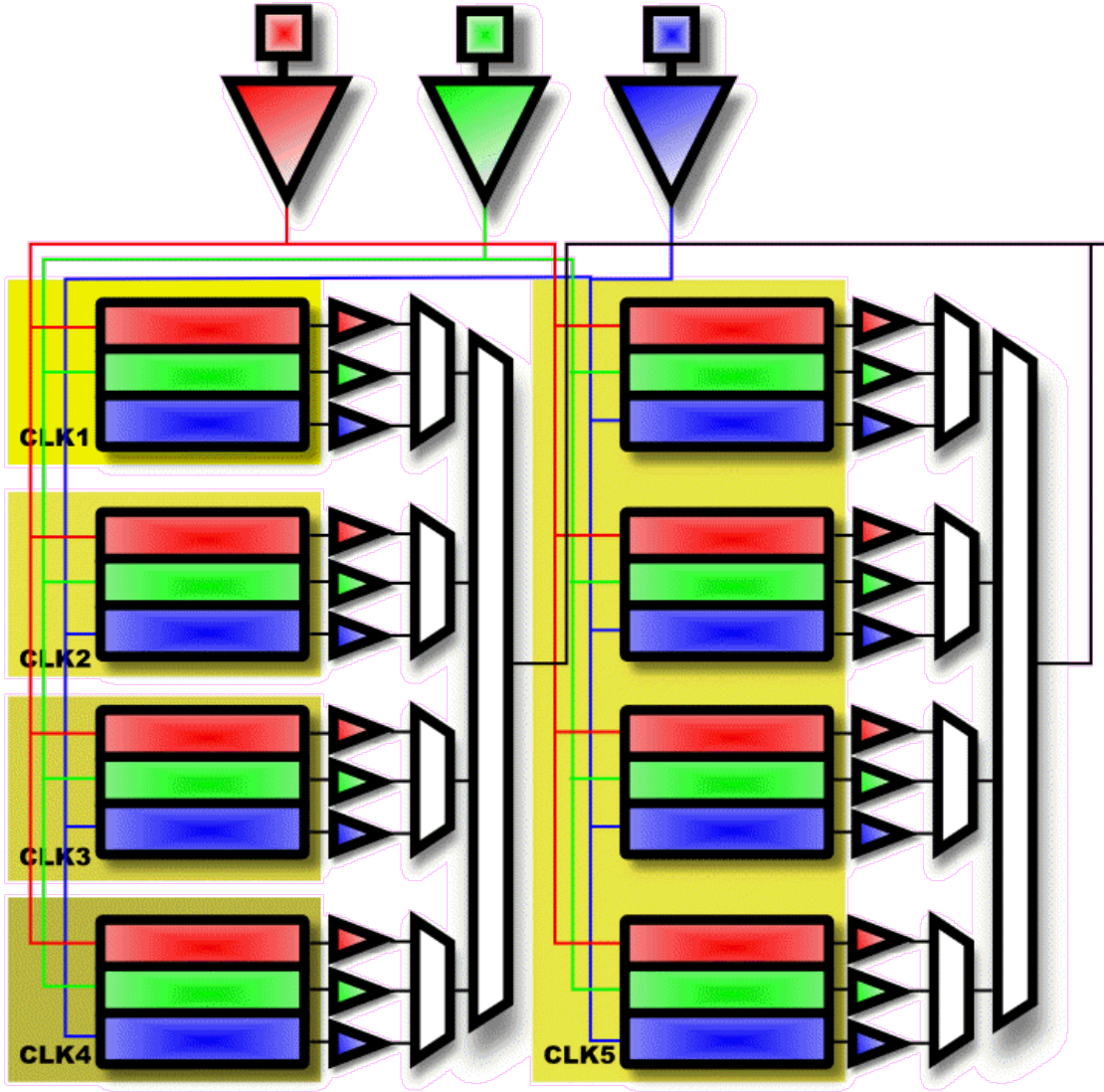
- Internal buffers connect input signals with all analogue memories blocks
  - Class AB OTAs
  - Rail-to-rail architecture
  - 35 MHz GBW

ASIC architecture



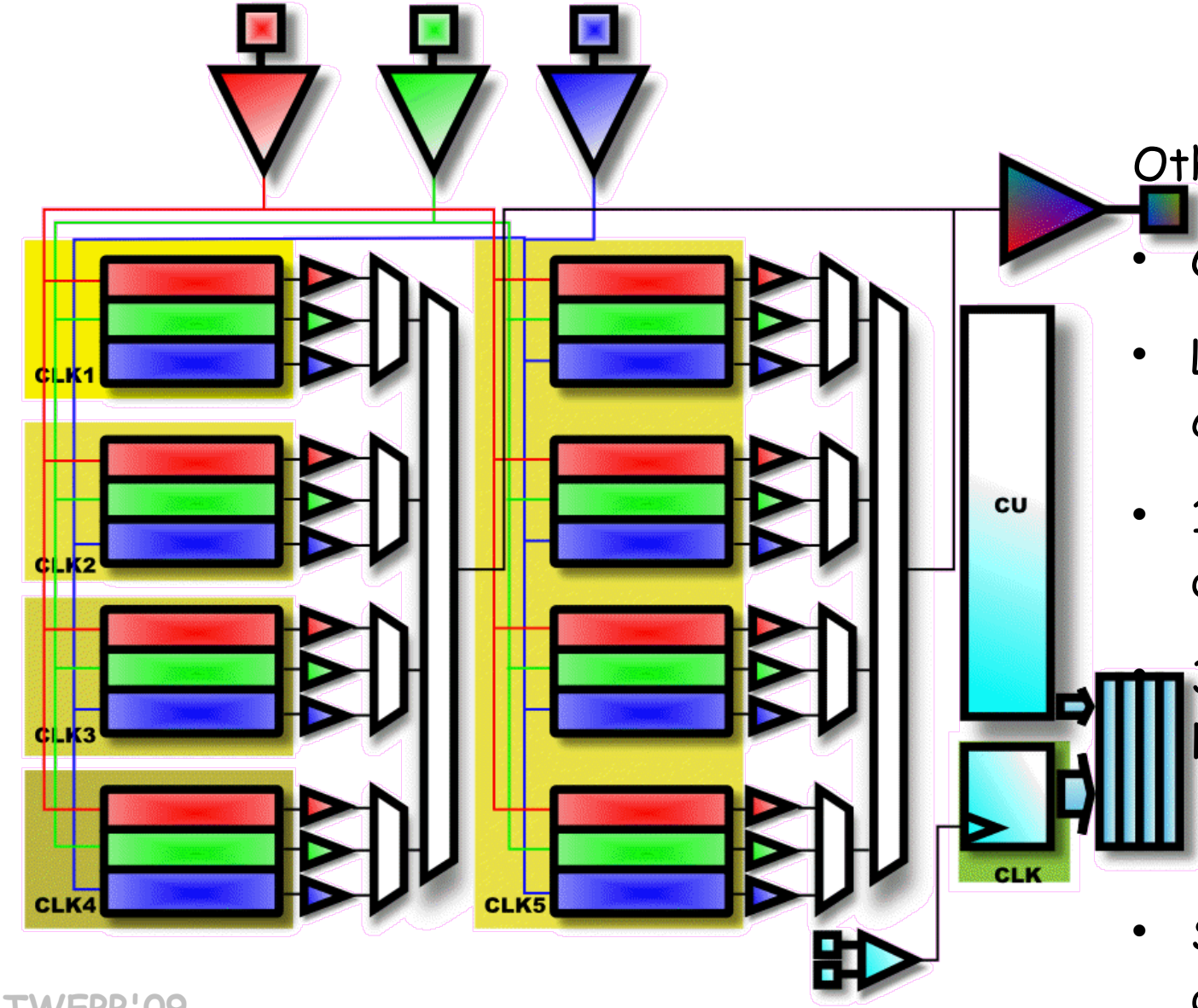
- Single analogue output pin
- Outputs of all memory banks are muxed together

ASIC architecture



- Single analogue output pin
- Outputs of all memory banks are muxed together
- Muxes operate depending on signal classification
  - Only one channel
  - All three stored channels

ASIC architecture



Other (digital) blocks:

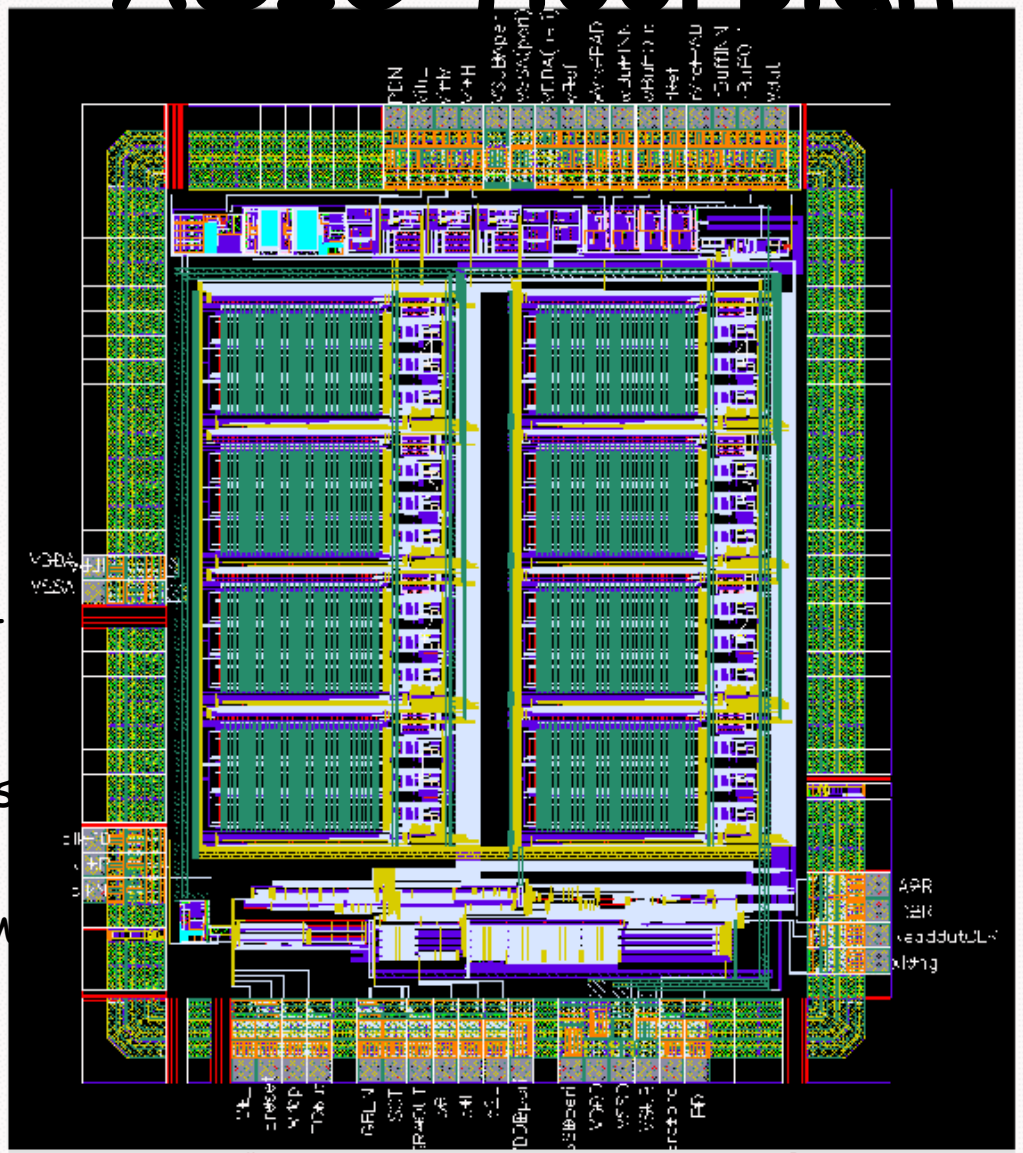
- Control unit
- LVDS 200 MHz clock buffer
- 17b synchronous digital counter
- 32b 4 levels digital FIFO
- Serializer for single digital output

Functional blocks

- Main blocks summary:
  - Analogue memory (voltage sampling unit):
    - 3 channels of 32 cells each
  - Input buffers
    - Class AB rail-to-rail architecture
    - Same topology also used for readout amplifiers
  - Asynchronous digital FIFO
  - Synchronous 17b counter
  - Internal references
  - Serializer module for single digital output

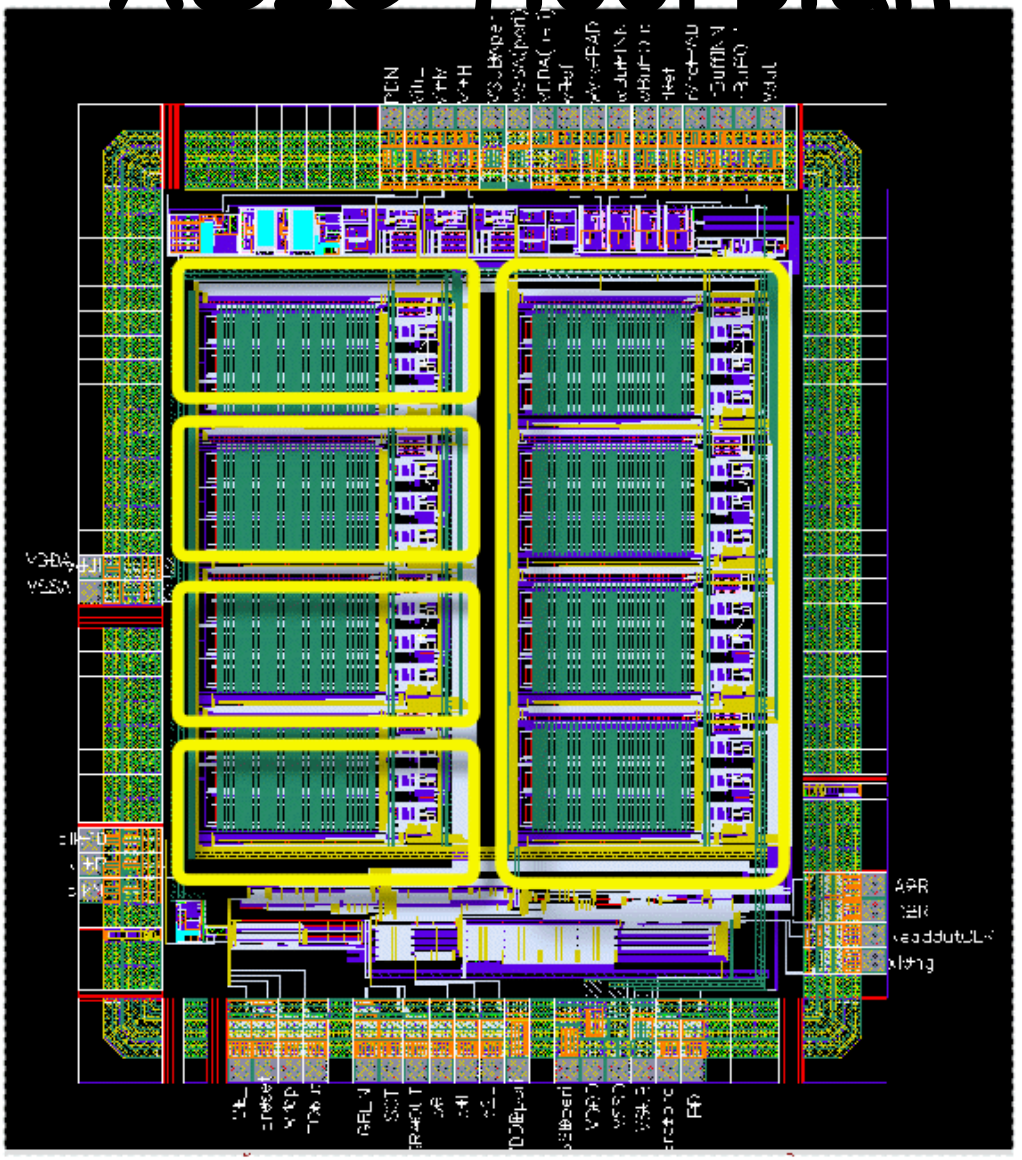
ASIC floorplan

- 0.35 um CMOS AMS process
- 3.3 V supply
- ~ 4 x 6 mm^2
- 44 pin JLCC ceramic package
- Full-custom mixed-signal design
- Std-cell library has been designed including async flow control cells



ASIC floorplan

- Analogue memory macrocells

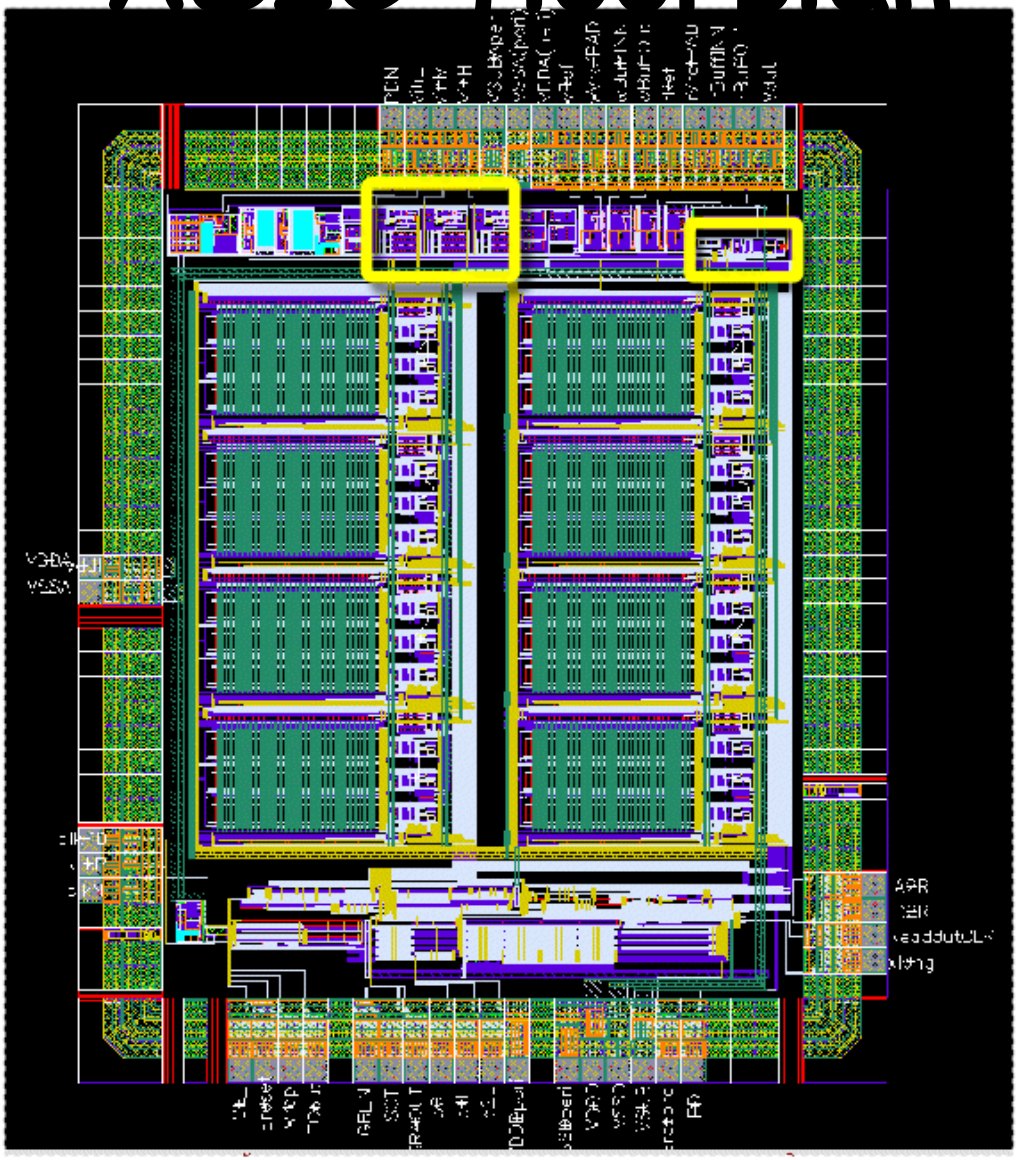


Each macrocell contains:

- 3x32 analogue cells
- write/read address units
- 200 MHz write
- TSPC clock scheme
- 20 MHz readout
- readout bank OTAs

ASIC floorplan

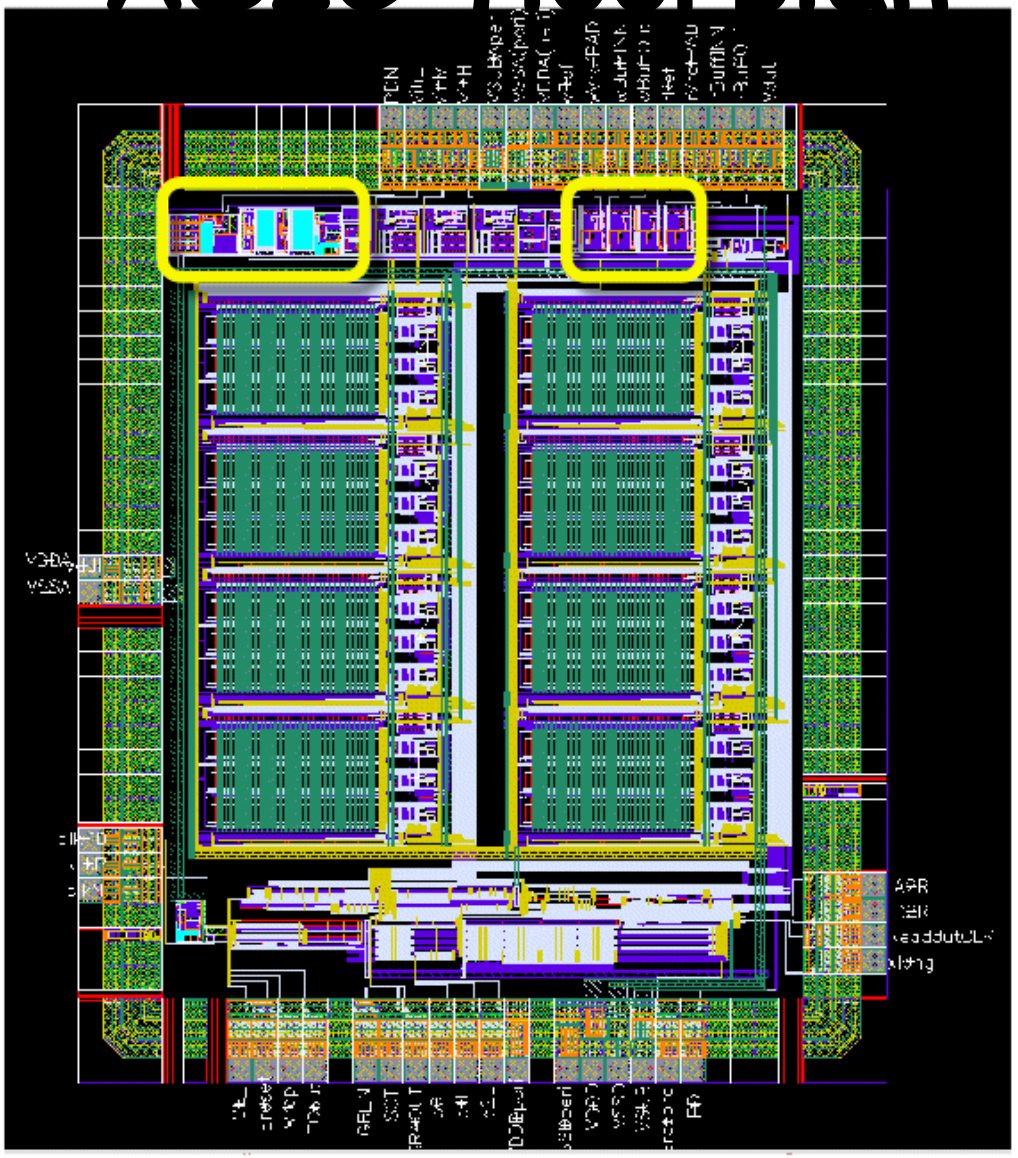
- Analogue memory macrocells
- Input and output buffers



- Same class AB architecture
- Rail-to-rail input and output stages

ASIC floorplan

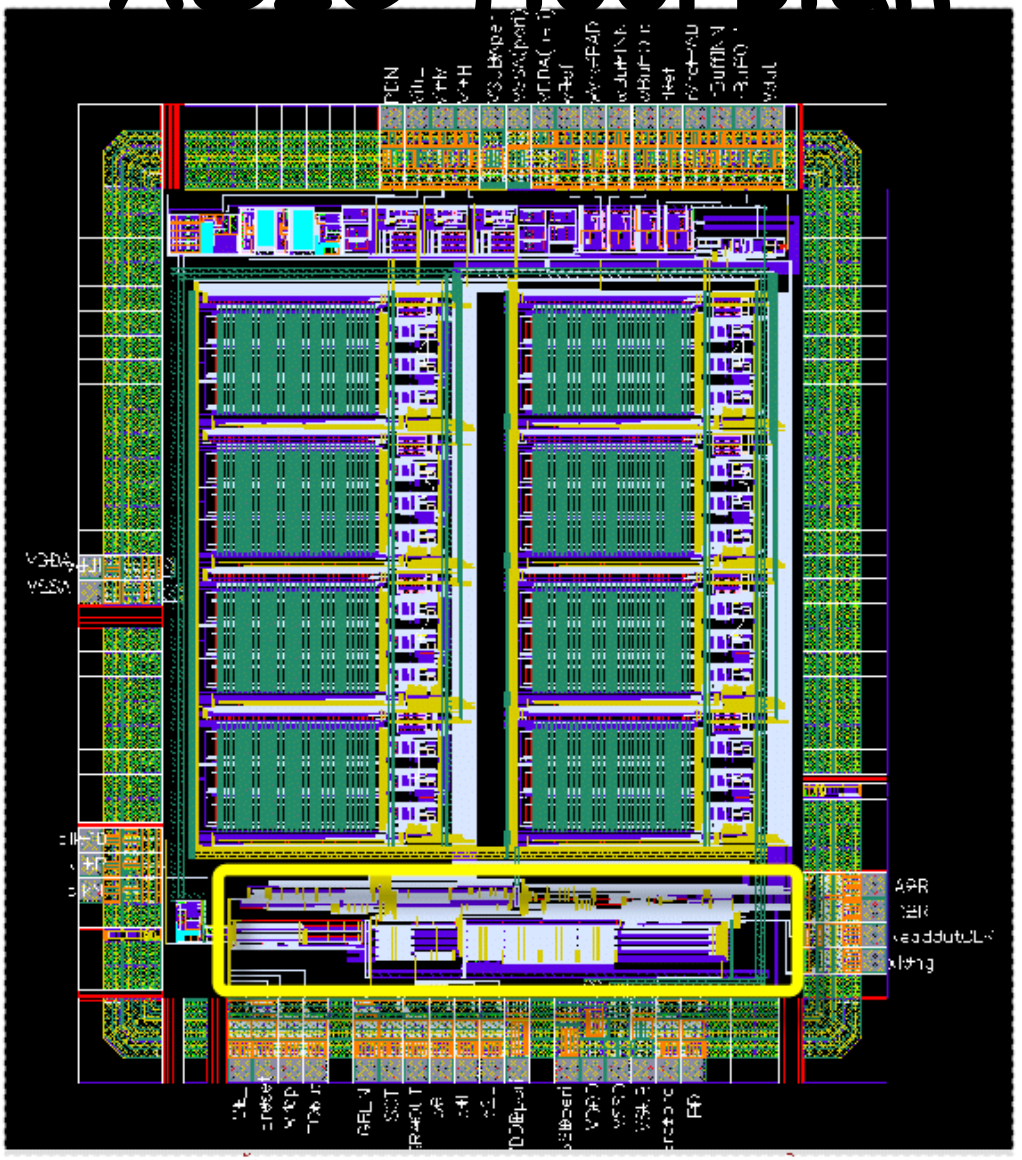
- Analogue memory macrocells
- Input and output buffers
- Internal bias and voltage references



- Library bandgap cell
- Internal voltage references
- 2 external capacitors needed

ASIC floorplan

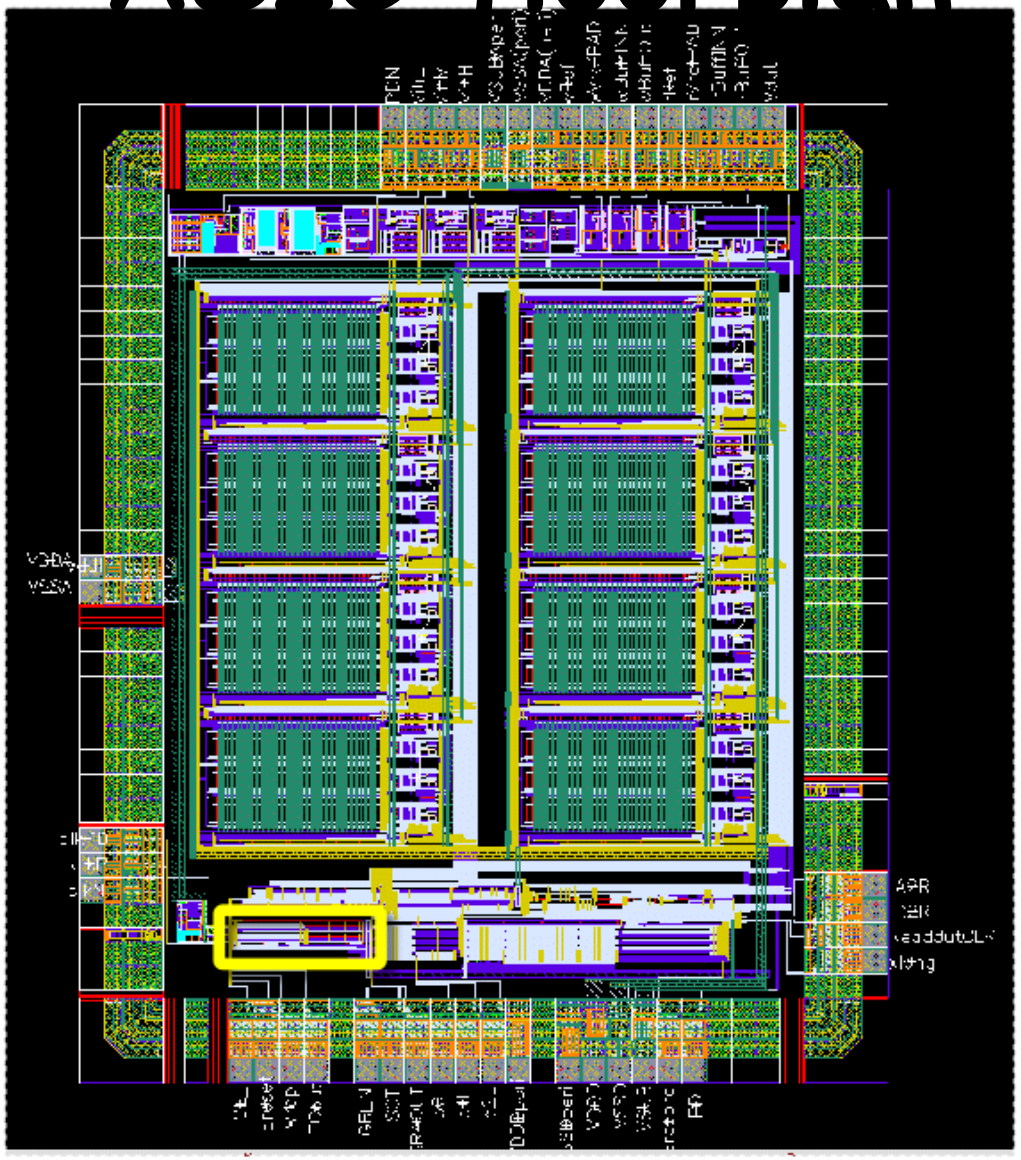
- Analogue memory macrocells
- Input and output buffers
- Internal bias and voltage references
- Control unit



- Digital asynchronous design
- Event-driven unit
- 200 MHz clock dispatched only to one memory block at time

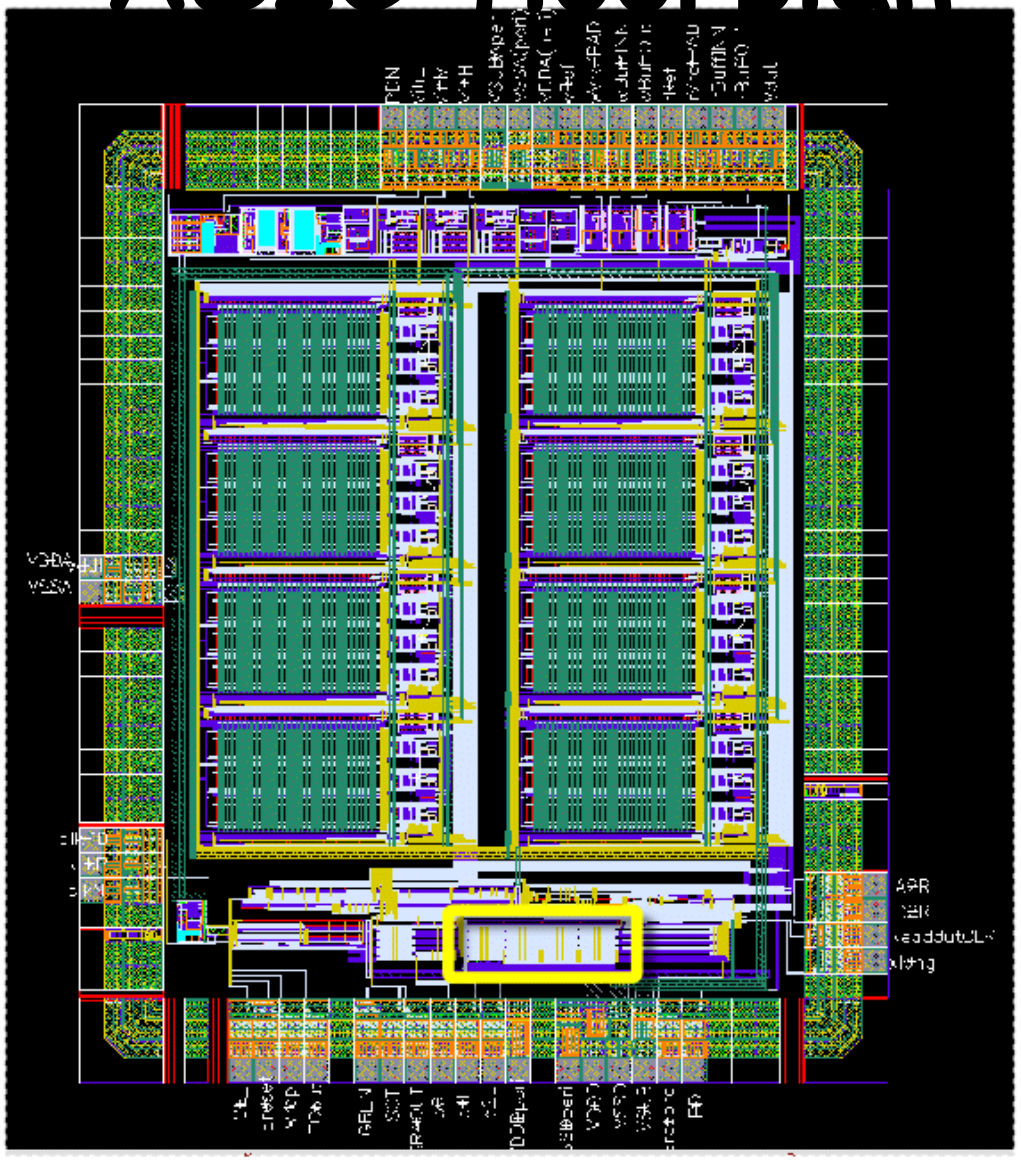
ASIC floorplan

- Analogue memory macrocells
- Input and output buffers
- Internal bias and voltage references
- Control unit
- 17b synchronous counter



ASIC floorplan

- Analogue memory macrocells
- Input and output buffers
- Internal bias and voltage references
- Control unit
- 17b synchronous counter
- Asynchronous digital FIFO



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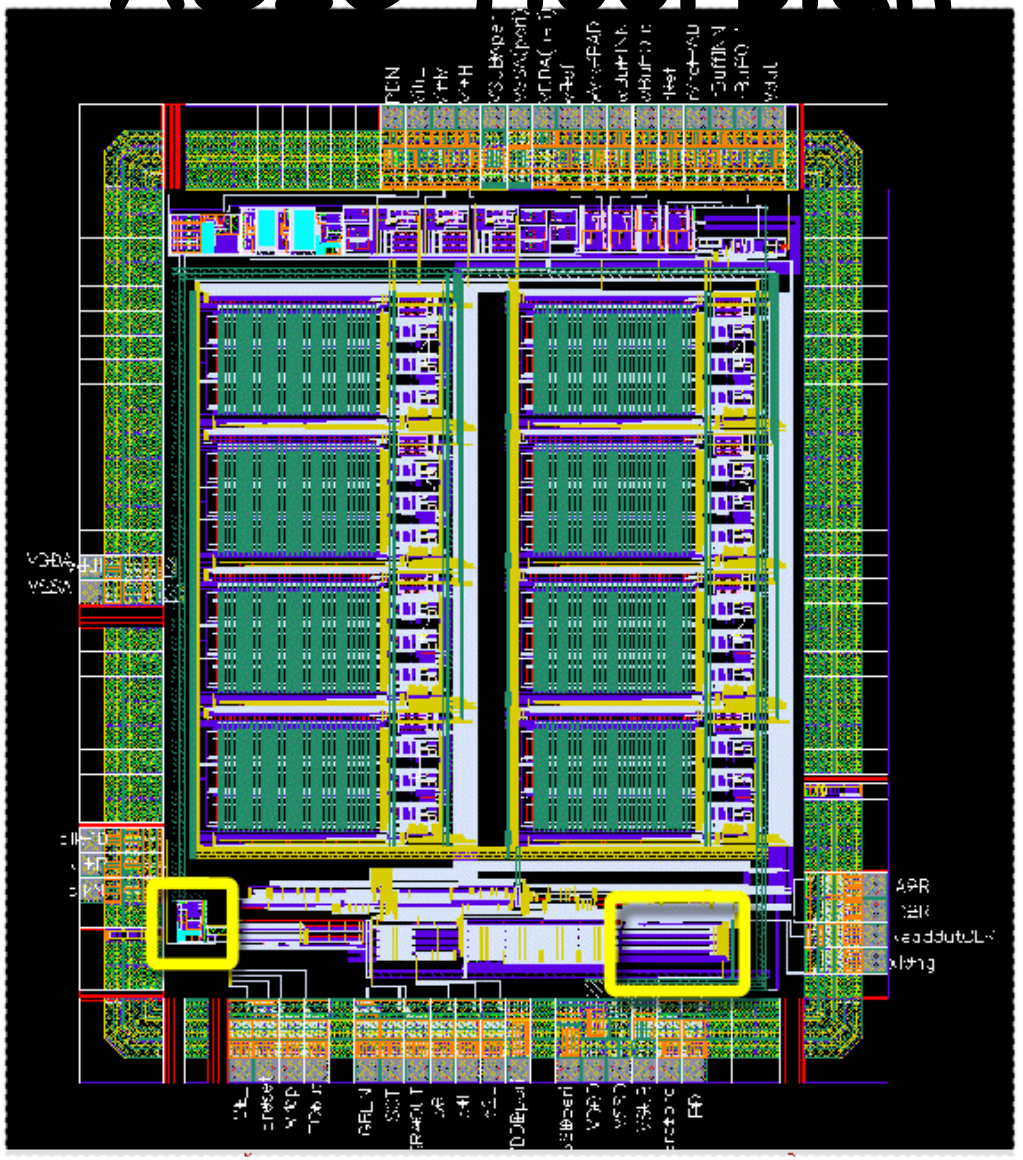
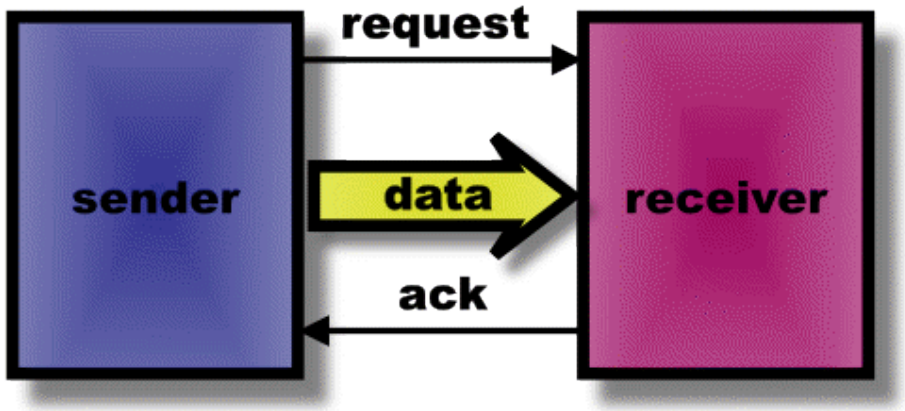
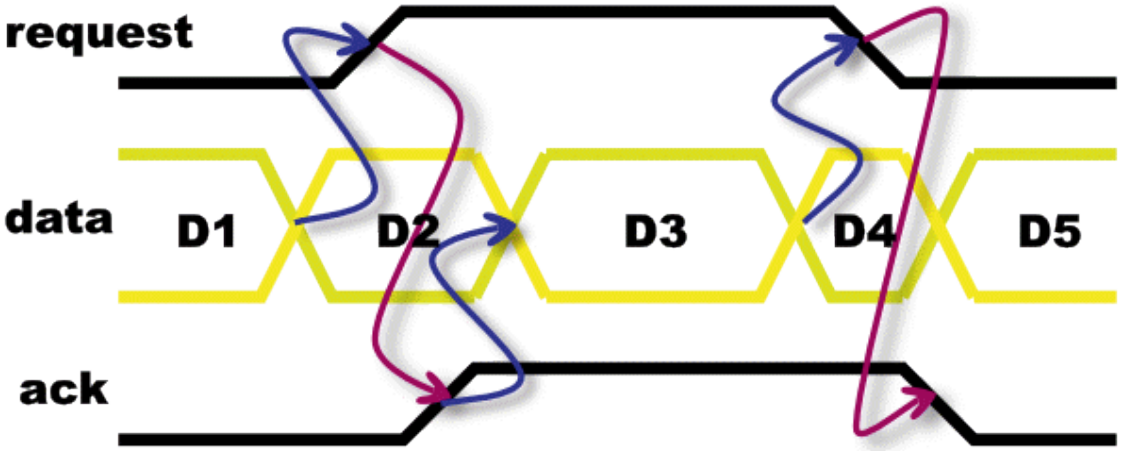


- Serializer
- LVDS 200 Mhz clock receiver

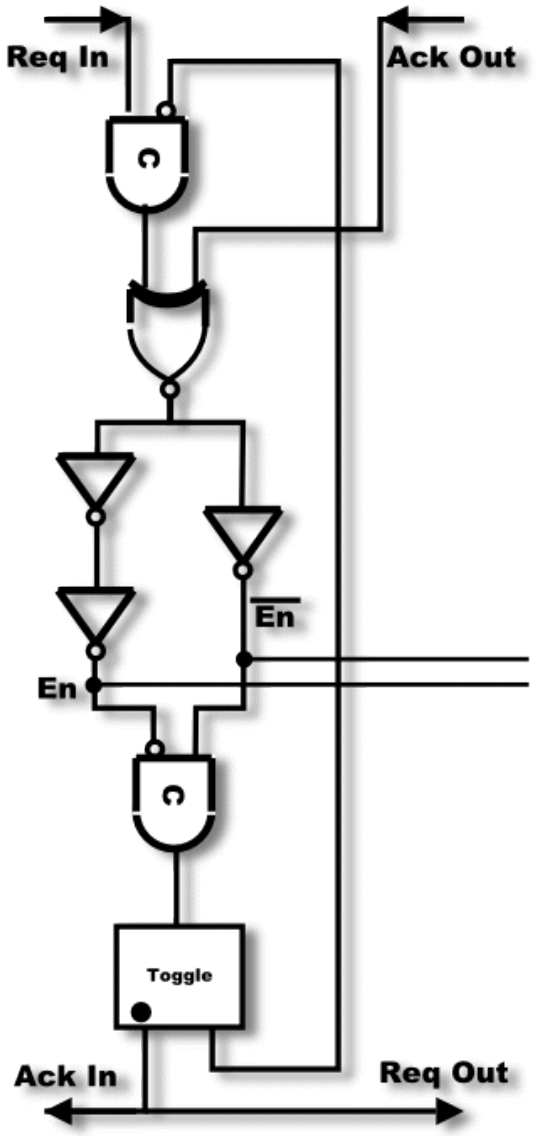
Asynchronous Control Unit: design issues





- Sender/receiver 2-phase protocol
- Data ready generates **request** action
- New data available only after **ack** action
- Event driven state machine: no global periodic clock
- Ease of composing async subsystems into larger blocks
- Basic synchronization element: C-Muller gate

Asynchronous Control Unit: design issues



- Sutherland's micropipeline based design
- Async ctrl logic basic unit
- Transparent latch style

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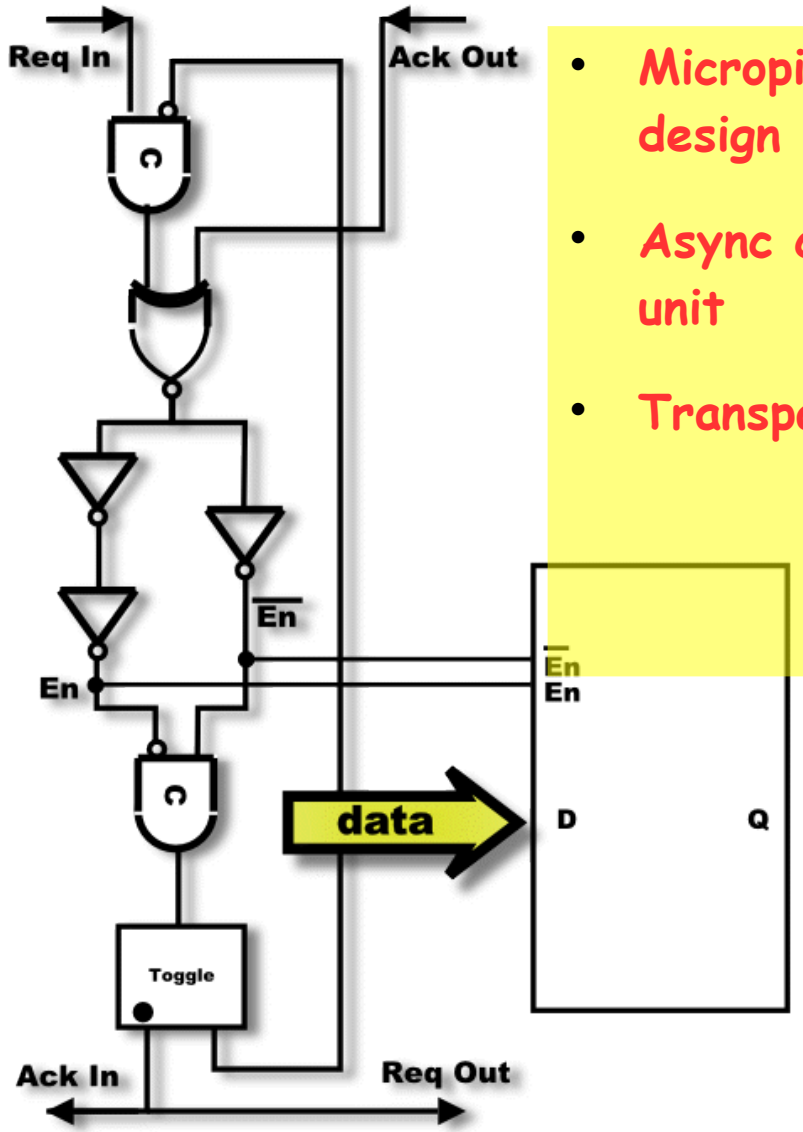

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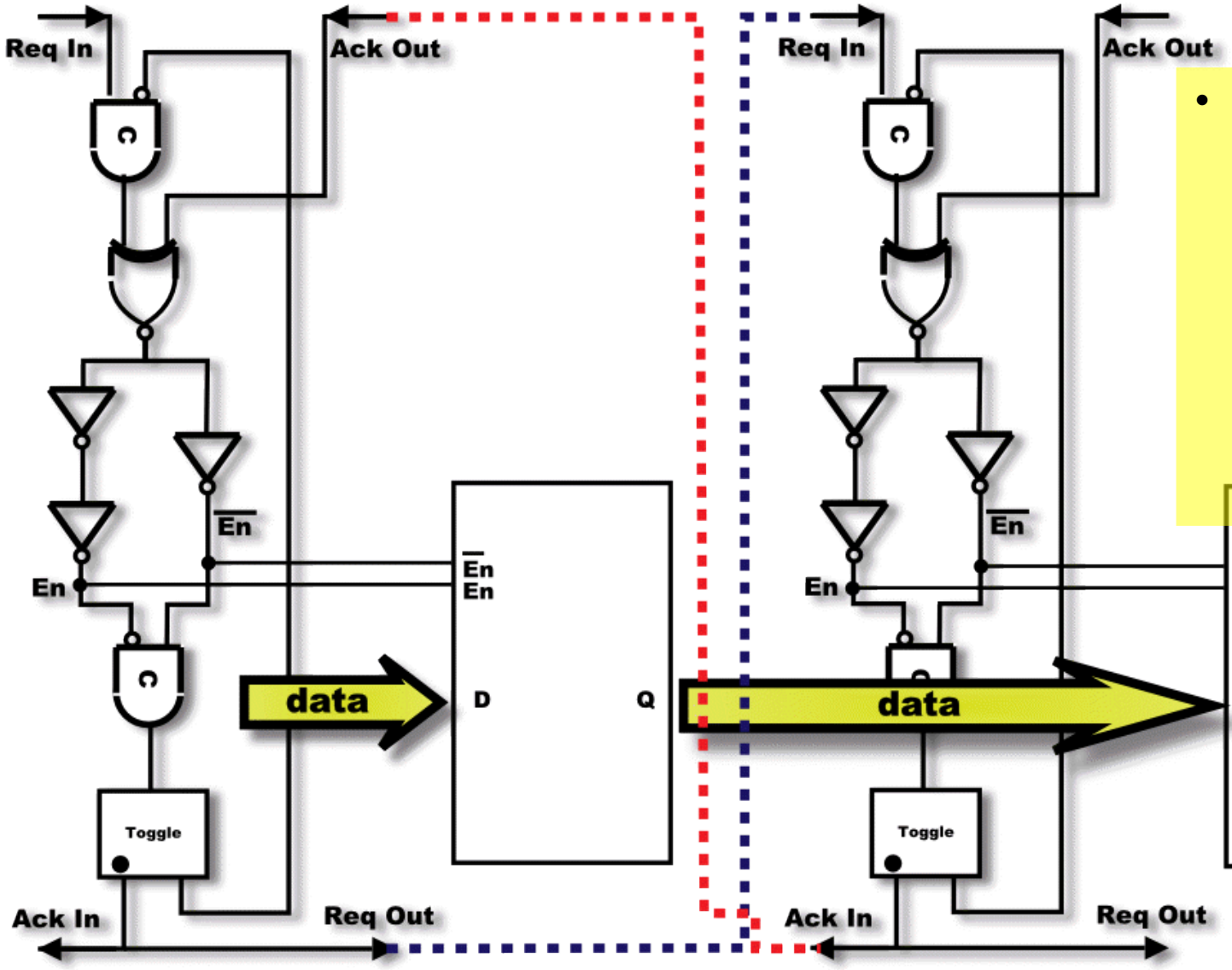
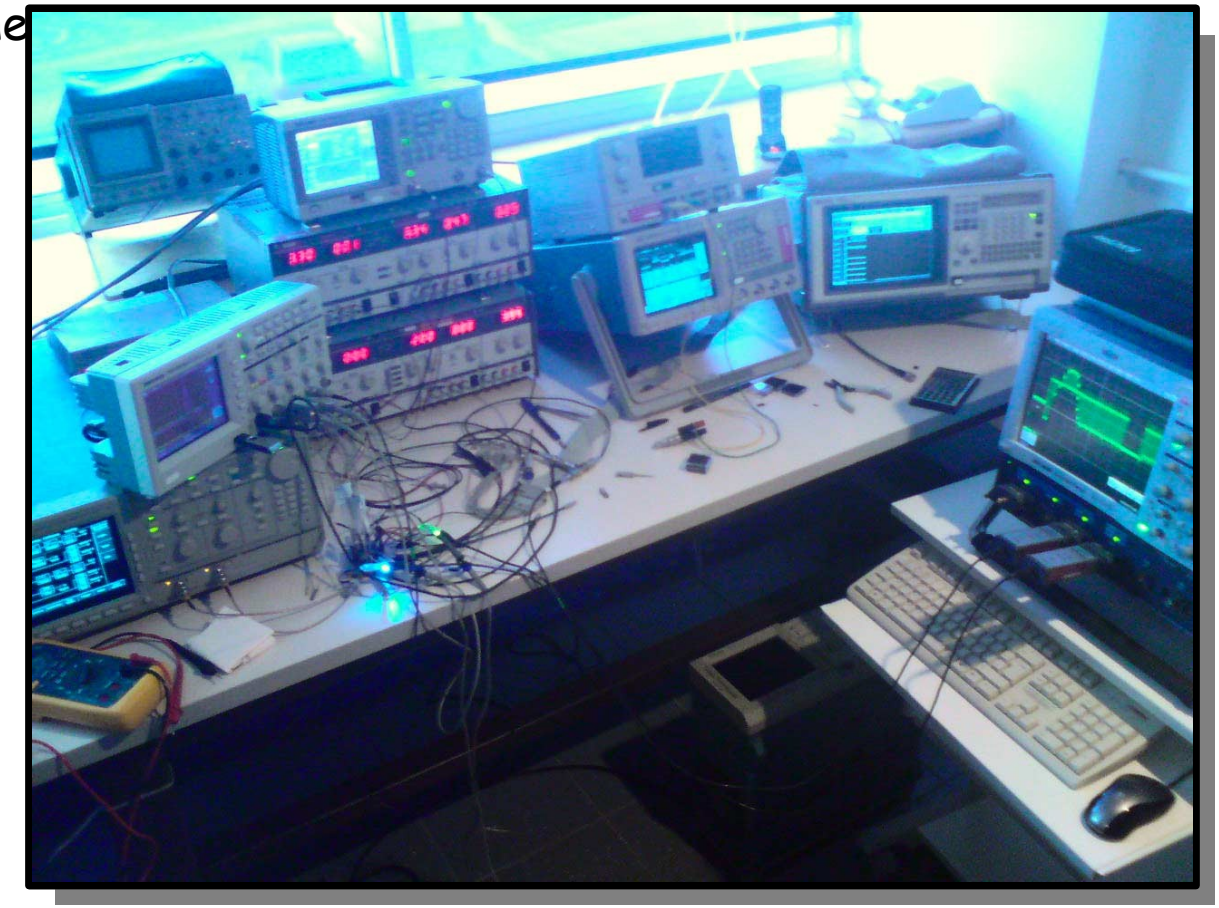


- Each pipeline stage manages its own synchronization with its left and right neighbors

Testing

- Packaged samples received in June '09
- Functionality test bench implemented at CPPM Marseille



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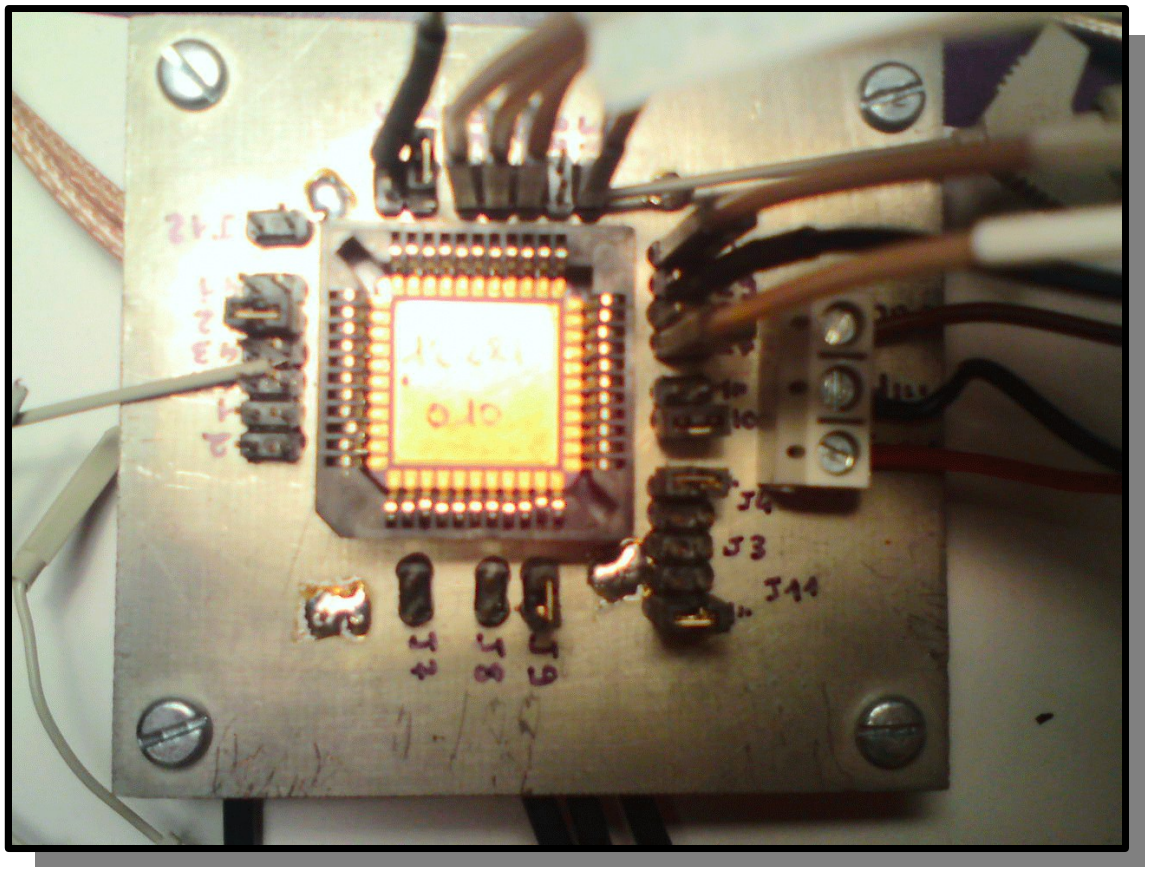
- (2 layers passive) test board
- Another board with ADCs, FPGA and PMT interface electronics under development at INFN Catania



Testing

- Packaged samples received in June '09
- Functionality test bench implemented at CPPM Marseille
- (2 layers passive) test board
- Another board with ADCs, FPGA and PMT interface electronics under development at INFN Catania
- Power supply consumption is less than 50mA for the analogue part

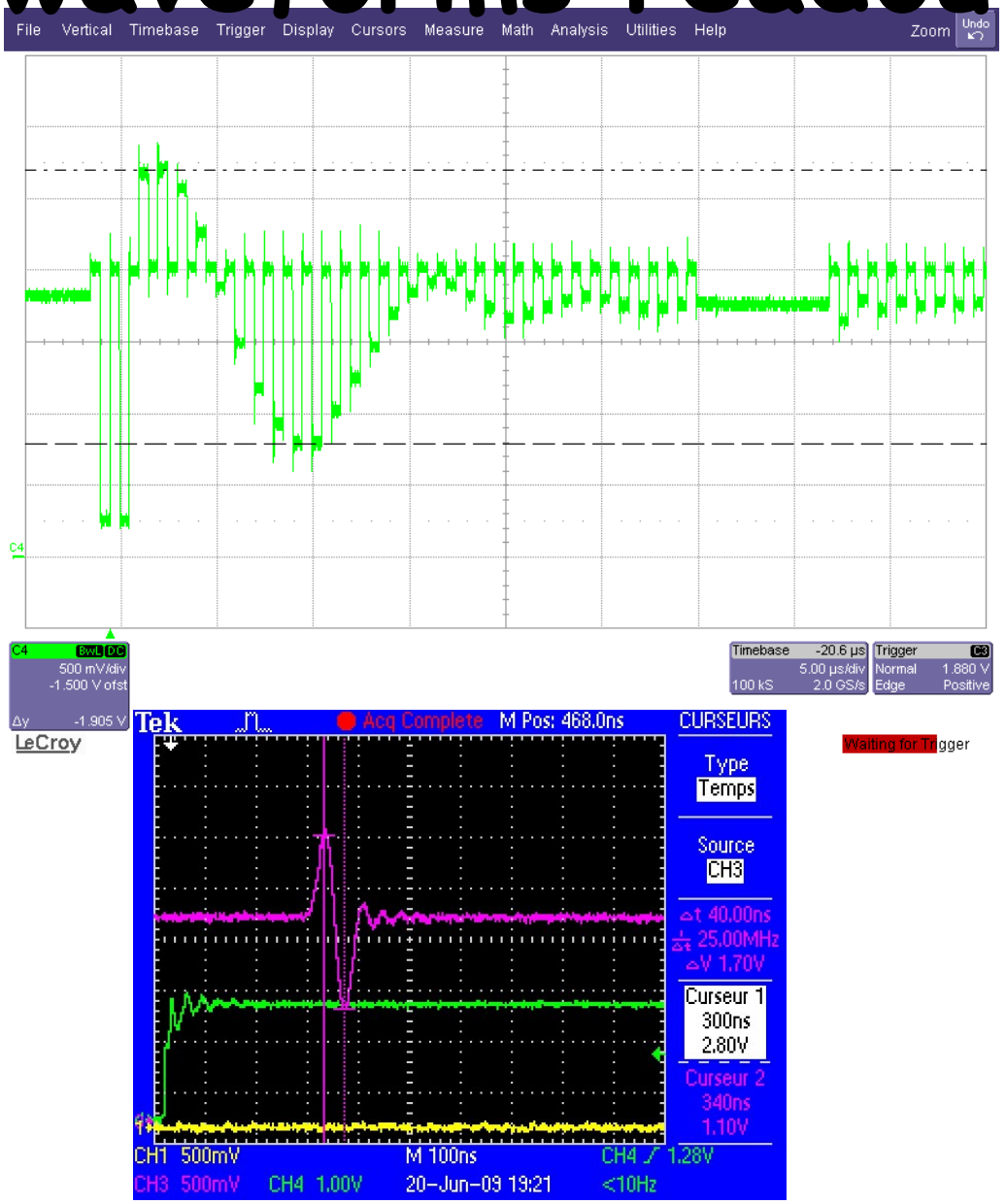
- Tests showed (analogue) output out of specs:
  - Can't be readout at 20 MHz rate

(preliminary) waveforms readout

- Top trace: SAS analogue output
- Bottom trace: input signal
- 10 ns delay from trigger to actual acquisition start
- Input signal is a 1.9Vpp rectangular pulse 50ns wide
- Acquisition rate is 200MHz
- Readout signal occupies 15 memory cells
- First 2 cells misbehave (internal skew design error)

(preliminary) waveforms readout

- Top trace: SAS analogue output
- Bottom trace: input signal
- Input signal is a 1.7Vpp full-period sinusoidal pulse 100ns wide
- 40ns peak to peak
- Acquisition rate is 200MHz
- Peak to peak readout waveform is ~8 memory cells
- First 2 cells misbehave (internal skew design error)



Summary and perspectives

- A front-end architecture for PMT signal acquisition in the framework of the KM3NeT consortium has been proposed
- A full-custom mixed-signal ASIC has been designed and 10 samples produced
- Preliminary tests showed readout rate is out of spec:
  - Further analysis traced back the problem to biasing design errors
- Tests also showed encouraging results for all ASIC functionalities
- A complete board with the ASIC, the PMT interface and signal classification electronics, the ADC and a FPGA is being developed at INFN Catania

Class AB OTA