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Smart Analogue Sampler for the Optical Module of a Cherenkov Neutrino Detector

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A transient waveform sampler/recorder IC has been developed and realized in AMS C35 technology to be used in the front-end of a neutrino detector. It is based around a switched capacitors array unit sampling its voltage inputs at 200MHz external clock rate and transferring them at its outputs at 1/10th of the sampling rate. This unit is replicated inside the ASIC providing 4 independent analogue sampling queues for signal transients up to 32 x 5ns and a fifth unit storing transients up to 128 x 5 ns. A micro-pipelined unit, based on Muller C-gates, controls the 5 independent samplers.

Summary

The use of an analogue sampler/recorder for the purposes of the front-end electronics of a Cherenkov neutrino detector has been exploited and demonstrated its effectiveness in detectors as ANTARES, Nestor and IceCube. The readout system of those detectors must provide the time-stamping of Single PhotoElectron (SPE) signals produced by photomultipliers while separating them from background and bioluminescence events which mainly contribute to the dead-time.
The solution presented has been tailored to sustain an event rate of short pulse (less than 160 ns) events in excess of 300 kHz with a negligible dead-time, with an amplitude of one SPE signals of about 570 mV, while still providing a mean to record longer photomultiplier events (640 ns + 160 ns maximum length).

The ASIC have three buffered analogue input channels and a single analogue output: a record of 32 samples is acquired after a rising edge is detected on its Signal Over Threshold (SOT) digital input. This also strobes the content of a 200 MHz internal counter inside a digital FIFO which stores it along with the reference to the analogue sampling queue holding the voltage values. After a fixed delay of 100 ns the status of the SOT pin is checked and a decision is made whether to end the sampling process within the 160 ns window, or continuing it, storing the samples into a larger unit holding a 640 ns time window.
At the end of the chosen sampling windows, the record formed by the counter time-stamp, the digital code classifying the three input signals and generated outside the ASIC and the stored samples for each of the three input channels, is put on hold and a Ready To Readout signal is issued on an output pin. Depending on the classification code, only one of the channels out of the three sampled ones will be multiplexed to the single analogue output pin for the external readout. The availability of four identical sampling units provides a buffer mechanism to the external data acquisition electronics able to deal with an event rate of SPE-like signals of about 300 kHz. The four units are independent the one from the other and the stored data could be readout from each unit while the next in the sequence is sampling its inputs. If a new rising edge is detected on the SOT pin when all 4 units still hold data (or a readout is being performed in one sampling unit) the three input channels are sampled by the fifth (longer) unit.

A full custom ASIC has been realized in a standard 0.35um CMOS technology: die area is about 12 mm2 and packaged samples should be available for testing by the end of May'09. The design is a full-custom mixed-signal circuit using switched-capacitors arrays and classAB rail-to-rail operational amplifiers in its analogue part, and Sutherland's micropipeline in the digital part: the supply voltage is 3.3V and the estimated power dissipation is less than 100 mW with a SNR better than 62 dB over 1V dynamic range.

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