The Control System for a new Pixel Detector at the sLHC

TWEPP 2009 - Topical Workshop on Electronics for Particle Physics

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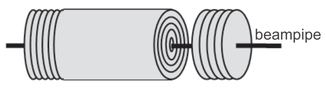
For the upgrade of the LHC, the sLHC (super Large Hadron Collider), a new ATLAS Pixel Detector is planned, which will require a completely new control system. To reduce the material budget new power distribution schemes are under investigation, where the active power conversion is located inside the detector volume. Such a new power supply system will need new control strategies. Parts of the control must be located closer to the loads.

The minimization of mass, the demand for less cables and the re-use of the outer existing services are the main restrictions to the design of the control system. The requirements of the Detector Control System and a first concept will be presented. We will focus on a control chip which necessarily has to be implemented in the new system. A setup of discrete components has been built up to investigate and verify the chip's requirements.

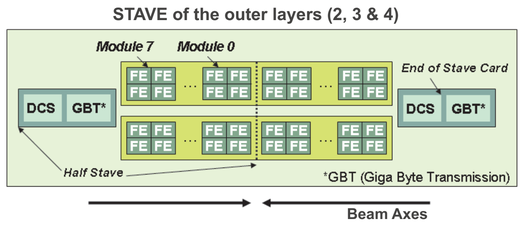
Pixel Detector for the sLHC

The planned Pixel Detector will be the innermost part of the ATLAS tracking system for the sLHC upgrade. Foreseen is a cylindrical detector around the beampipe with up to five layers and five disks per endcap.



The smallest unit on which the detector control system can act is a detector module. It is mounted on staves in the barrel and on wedges in the disk region.

STAVE of the outer layers (2, 3 & 4)



2 single sided staves sandwiched together back to back

Layout:
- 32 modules/stave, respectively 24 modules/stave in layer 1
- 4 FE chips/module, respectively 1 FE/module in layer 0
- Powering schemes:
  I. Serial Powering
  II. Parallel Powering with 2 DC-DC stages

DCS requirements

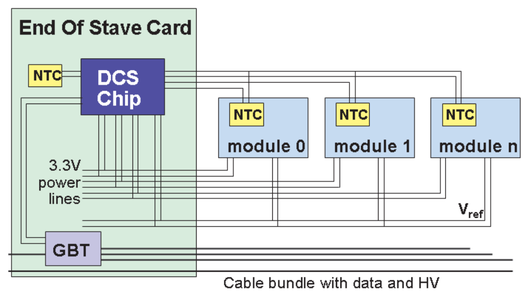
For the new Pixel Detector a low material DCS is needed with the following requirements:

component	to be monitored	to be controlled
Detector Module	HV: voltage & current	voltage setting On/Off
	LV: voltage & current	voltage setting On/Off
	temperature	
End Of Stave Card	voltage & current	voltage setting On/Off
	temperature	
		reset
On-detector Opto Transceiver	voltages & currents	voltage setting On/Off
	temperature	
		reset
Environment	humidity	
	temperature	

For each item one has to define:
- the granularity
- the location of data processing (e.g. on-detector or in the control room)
- the reliability
- the lifetime (e.g. permanent or on request)

DCS for DC-DC powering

In this powering option the modules of the half stave will be powered in parallel with a 2 stage DC-DC conversion, one inside the front end chips, one further outside.

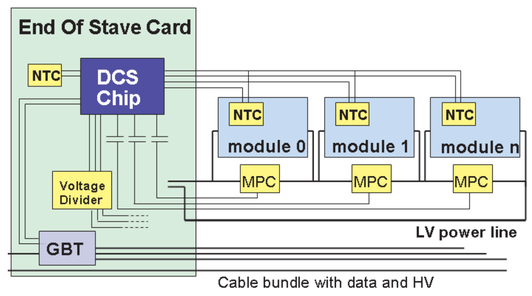


On-detector DCS:
- monitoring of LV per detector module
- monitoring of V_{ref}
- monitoring of temperature per detector module
- monitoring and reset of GBT
- temperature of the End of Stave card

DCS lines:
- (number of modules + 1) for temperature monitoring

DCS for serial powering

The modules of one group (e.g. half stave) are powered serially by one common current source.



On-detector DCS:
- monitoring of LV per detector module
- monitoring of temperature per detector module
- steering of bypass

DCS lines:
- (number of modules + 1) lines for the temperature monitoring
- (number of modules) lines for the bypass control

The Module Protection Chip (MPC) developed by Bonn University can bypass the detector module and guarantees an overvoltage protection.

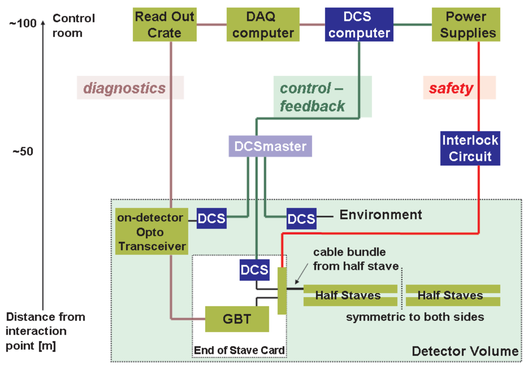
Pixel DCS architecture

The new Detector Control System consists of three paths:

Diagnostics
On request detailed data will be merged into the data stream.

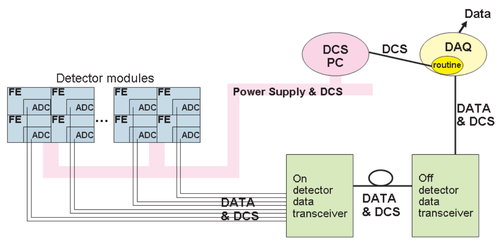
Control
The control/feedback must be available for all use cases and does not rely on the functionality of the readout data path.

Safety
The interlock system is always active and will be built up with an independent hardware system located outside the detector volume.



Diagnostics

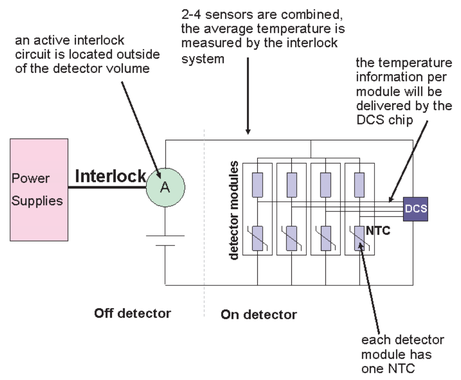
Optional additional data will be provided with high granularity for debugging, like the temperature and the LV per FE chip.



- the additional DCS values can be merged into the data stream
- a software routine inside the DAQ system has to provide the DCS data for the DCS computer
- the diagnostics information will only be available, if the FE's are already properly configured

Safety

As high temperatures can cause irreparable damages to irradiated detector modules, an interlock system is needed.



The interlock system is always active and completely independent. To guarantee a stable operation it is a hardwired system without any software or initialisation routines.

Control & Feedback

In this path all important detector information are delivered with a high reliability. The information are available for all use cases and will be processed at the power supplies or directly at the detector modules by a DCS chip.

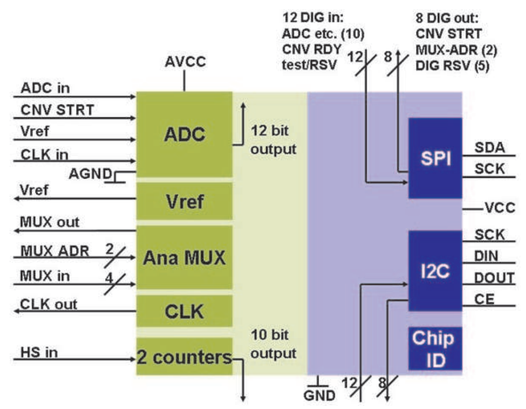
DCS chip overall requirements:
- radiation hard up to 1.3×10^{16} n/cm^2, 570MRad
- low power consumption (for operation without cooling)

DCS chip to the outer world:
- power and data (twisted pair) will have separate lines
- separate voltage divider in case of serial powering
- communication protocol must be compatible with long cables

The DCS chip has to handle 3 different tasks (see DCS architecture):
- control of the modules and of the End of Stave card
- control and reset of the optical link
- readout of the environment & cooling sensors inside the detector

DCS prototype chip

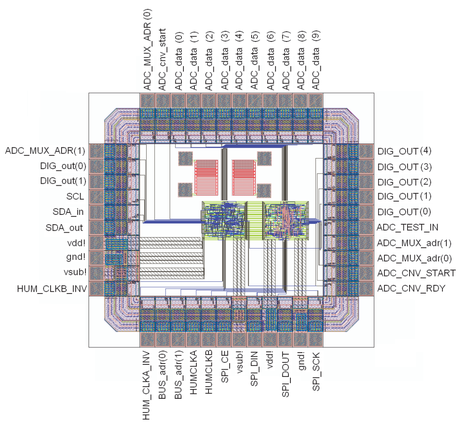
The functionality of the DCS chip prototype is shown in the following block diagram:



DCS chip requirements:
- SPI or I²C Interface (need a protocol with minimal lines)
- differential in/out signals
- minimum 35 ADC channels
- 10-12 bit differential ADC
- minimum 17 digital outputs
- reference voltage for the ADC
- chip ID
- two 16-bit counters for humidity measurement

Submission of DCS prototype chip

The first prototype of the digital part for the DCS chip is submitted in sub micron 350nm technology.



- for debugging all in/out lines are routed to the outside
- size per core: 0.3 x 0.3 mm²
- 44 pads

Components of the digital DCS chip prototype:
- SPI Interface with a bus address
- I²C Interface with the classical I²C protocol
- 5 digital outputs
- ADC inputs
- 2 resistors to test analog components
- 2 x 12 bit counter

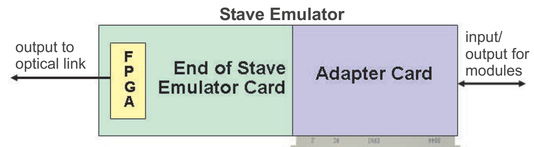
Tests foreseen with the prototype:
- verification of the SPI and I²C protocol
- test of possible cable lengths
- built up of a DCS network
- control of external ADC
- test of outputs
- readout of humidity sensor
- integration into system test setup (COBOLT)

COBOLT

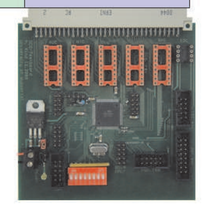
The **CO**ntrol **BO**ard for the stave emu**L**a**T**or is a DCS test setup to study different options and system aspects of a powered stave.

The stave emulator developed by Bonn University is a setup to investigate and understand a complete Pixel stave system.

Stave Emulator



COBOLT
- ATmega640V
- 10 bit ADC, 16 channels
- several plugins, e.g. for voltage divider



COBOLT tasks:
- check continuously compatibility of the DCS system to the overall stave design
- verify LV monitoring per module without additional sense lines

Results:
- bypass control for serial powering is working