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The Control System for a new Pixel Detector at the sLHC

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For the sLHC upgrade a new ATLAS Pixel Detector is planned, which will require a completely new Control System.
The requirements, a first concept and a layout will be presented. We will focus on a control chip which necessarily has to be implemented in the new Detector Control System. A setup of discrete components has been built up to investigate and verify the chip's requirements.
First measurements with this setup will be presented.

Summary

The detector control system (DCS) of the pixel detector has to cover three main tasks. It should ensure the safety of the detector at any time. For all use cases (production, installation, commissioning, calibration, tuning the detector or parts of it) the operator must be provided with tools for control and he should receive feedback. On request the operator should be supported with more detailed information for diagnostics.

Based on these requirements a concept for the Control System for a new pixel detector has been developed with respect to balance between the granularity, the level of reliability and the reduction of radiation length. As the control system depends strongly on the powering scheme of the detector, its development handles two powering options: the serial powering and the DC-DC conversion.

To cover all these needs, the system is structured into different parts. For reliability issues, the interlock path is a completely independent circuit which ensures the safety of the detector at all times. Information for debugging is provided by monitoring values which can optionally be transmitted by the front end electronics via the data path. Control and feedback is required for the supply voltages of the detector modules, and the status of the end of stave controller and of the opto electrical receiver units. The front end unit of this path will be a dedicated DCS chip.

To avoid the routing of all cables to the outside, the DCS chip has to be designed to measure the DCS values as close as possible to the load and to the control units where necessary. The goal is to have one DCS chip design which can fulfill all measurement and control tasks. The chips will be located at various positions in the pixel package for their
different purposes.

A setup of discrete components, the COntrol BOard for the stave emuLaTor (COBOLT) has been built up to investigate and verify the chip's requirements. Various measuring circuits were realized and different communication protocols studied. First results were presented.

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