High-Speed Serial Optical Link Test Bench Using FPGA with Embedded Transceivers

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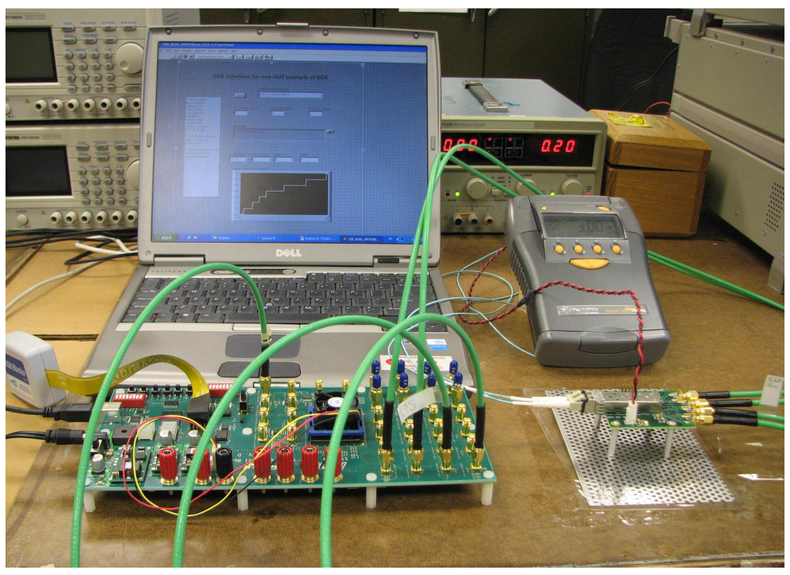
Introduction

Serial optical data transmission provides a solution to High Energy Physics experiments' readout systems with high bandwidth, low power, low mass and small footprint. It is widely proposed to be used in detector upgrades for SLHC. Commercial FPGAs with embedded multi-gigabit transceivers have become readily accessible. Altera's Stratix II GX family and Xilinx's Virtex 5 FXT family offer comprehensive data interface designs that operate up to 6.5Gbps. And the newest Stratix IV GX and Virtex 6 push the serial transceiver rate up to 10Gbps.

We develop a test bench based on Altera' s Stratix II GX Transceiver SI Development kit. Demonstrate it on a Point-2-Point serial optical link. And compare it with a stand alone Bit Error Rate Tester. 8b/10b protocol is implemented and its effects studied. Single bit flip will affect two code-groups and results in multiple errors detected. Word error is a more accurate measure in this scenario.

Test Bench



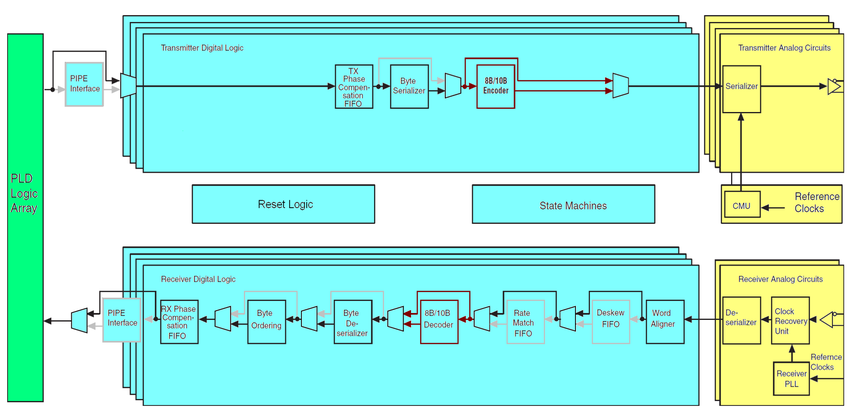
Signal Integrity

- Above eye diagram shows the near-end transmitter output of a common configuration: 5Gbps serial data rate, 800 mV differential voltage, no pre-emphasis, PRBS-7 data pattern at room temperature.
- Electrical signal loopback is error free for three days.
- Transmitter rise/fall time, jitter output, jitter transfer and receiver jitter tolerance data are available for link budget planning.

Characteristic

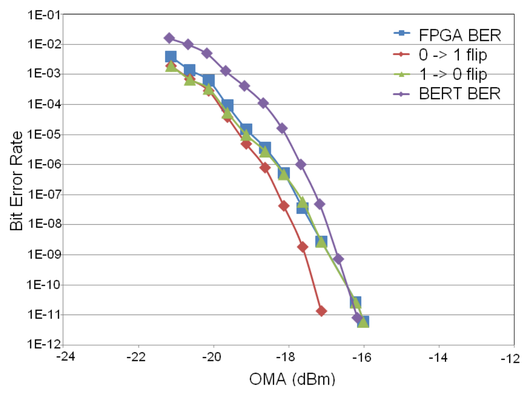
- The Stratix II GX transceiver is configured in basic mode. Dynamic reconfiguration supports switching of analog setting at run-time.
- Double widths data path is used to support data rate over 3.125Gbps. And byte serializer is needed to allow FPGA core to run at adequate frequency.
- The word aligner detects word patterns, aligns word boundaries and signals synchronization. Then the bit error rate test is enabled.
- A pseudo-random binary sequence (PRBS) generator and checker is implemented for the bit error rate test. Test pattern is implemented in polynomial shifters.
- The error checker uses the incoming data as seed to generated expected output pattern, until pattern match is declared. The checker then switches to internal seed.
- PC user interface through USB is coded in LabVIEW to enable feature settings and data analysis settings .

Embedded Transceiver



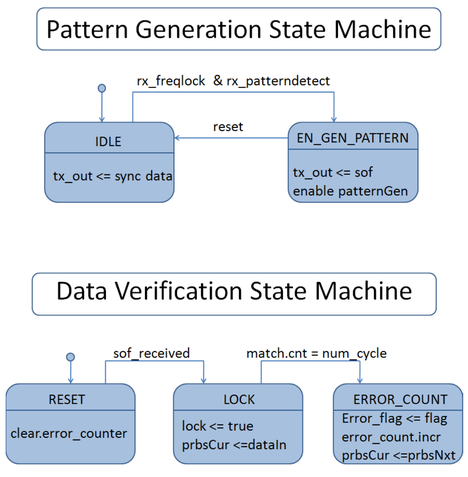
- Above diagram shows the use case of the transceiver block in basic mode with and without 8b/10b coding.
- When 8B/10B is not used, data bus on PLD side is 40 bit wide. When 8B/10B is used, data bus on PLD side is 32 bit wide.
- Basic clock of 156.25MHz is enabled to generate serial references.

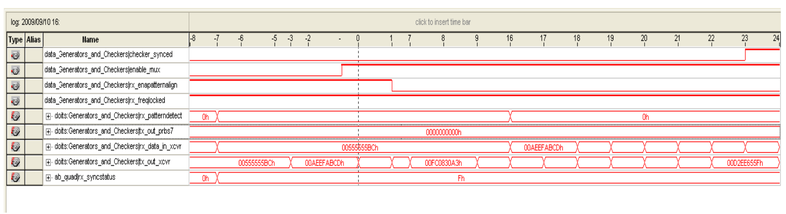
Basic BER



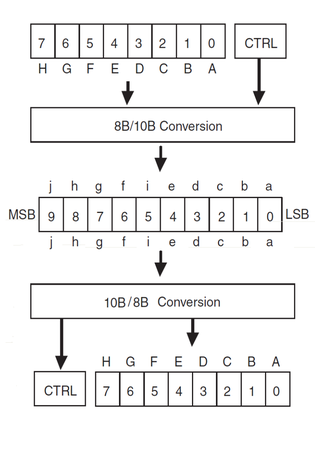
- A variable optical attenuator is inserted in the fiber loop to induce transmission degradation.
- The above error rate measurement compares results of the FPBA BERT and than of a commercial BERT. It also shows that there are more 1 to 0 bit flip than 0 to 1 bit flip at lower error rate in this degradation scenario.

PatternGen & ErrorChk





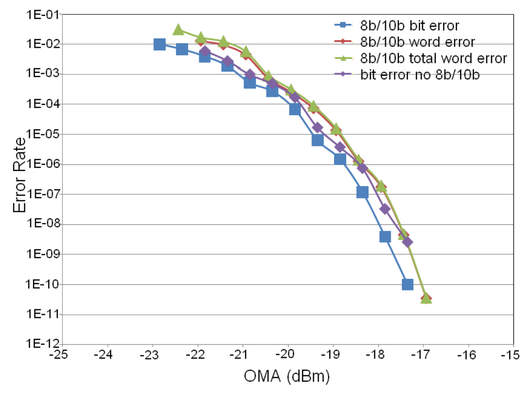
8B/10B



- The 8B/10B coding is used by many protocols such as Fiber Channel, Gigabit Ethernet, PCIe and XAUI.
- The 8B/10B coding algorithm achieves: DC balanced data stream; Sufficient level transitions; Unique code groups
- Stratix II GX devices support two dedicated 8B/10B encoders in each transceiver channels. It works in cascade mode and complements the word aligner to achieve boundary synchronization.

Stream	Code-group RD		RD	Code-group RD		RD	Code-group RD		RD
Transmitted code-group	–	D21.1	–	D10.2		–	D23.5		+
Transmitted bit stream	–	101010 - 1001	–	010101	–	0101	–	111010 + 1010	+
Received bit stream	–	101010 - 1011[a]	+	010101	+	0101	+	111010 +[b] 1010	+
Received code-group	–	D21.0	+	D10.2		+	invalid code-group[b]		+[c]

Word Error



- In 8B/10B coded transmission, a single bit flip in the serial data stream may affect two code-groups as exampled in the table on the left.
- The propagation of errors is eventually prevented by nonzero disparity blocks. Although the delay is uncertain depending on transmitted data.
- When a code/disparity violation is detected, the decoder output is not valid. Hence it makes more sense to count word errors instead of bit errors.
- The above error rate measurement shows that more word errors were detected than bit errors when the 8b/10b transmission degrades. It also confirms that 8b/10b error rate is confined and not much worse than none coded transmission.

Expansion

- Additional features of error logging is developed and will be used to investigate timing distribution of erroneous events during link degradation.
- At higher data rate, 64B/66B coding is preferred and will be implemented in place of 8B/10B coding.

Summary

- A high-speed serial optical link test bench using FPGA with embedded transceiver is demonstrated. This test bench is proposed to characterize physical layer components and to verify link bit error performance.
- The test bench consists of a PRBS generator and detector, implements on Altera's Stratix II GX development kit, with configurable embedded transceiver and provides PC LabVIEW interface for automation and control.
- 8B/10B protocol is implemented and studied. Although bit error can spread into multiple code groups, word error rate is contained by disparity blocks.

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