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High-Speed Serial Optical Link Test Bench Using FPGA with Embedded Transceivers

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Serial optical data transmission provides a solution to High Energy Physics experiments' readout systems with high bandwidth, low power, low mass and small footprint. It will commonly be used in detector upgrades for the SLHC. In the meanwhile, commercial FPGAs with embedded multi-gigabit transceivers have become accessible. We develop a test bench with such a device at its core to verify link configurations, evaluate radiation tolerant components and automate test procedures. The prototype's applications in irradiation tests and characterization tests such as online data analysis, bit error rate (BER) sensitivity, jitter extraction and bathtub curve are discussed in detail.

Summary

New High Energy Physics experiments impose ever more stringent demands on bandwidth and radiation tolerance of optical transmission links. The rapid increase in number of data channels and transmission speed justifies the exploitation of mature commercial silicon technologies. FPGAs with embedded multi-gigabit serial transceivers (MGT) such as Altera's Stratix II GX family and Xilinx's Virtex 5 FXT family offer comprehensive data interface designs that operate up to 6.5Gbps. The newest Stratix IV GX and Virtex 6 push the serial transceiver rate up to 10Gbps. A reference link deploying this proven solution serves as a configurable test bench as well as a custom design baseline. It can be used to verify various radiation tolerant optical links and test their components that are under development for detector upgrades for the SLHC. In this paper, we present a hardware system of commercial FPGA with MGT and a firmware/software platform to support its application in link characterization tests and component irradiation tests. The system's most basic function is BER testing. We investigate links using the FPGA test set with various optical transceiver modules and compare to links using a standalone Anritsu MP1763/4 bit error test set. The results show no significant discrepancy. Automated sensitivity test is also performed where a Labview program interfaces with the FPGA and a variable optical attenuator to obtain the BER vs. optical modulation amplitude curve. Single-event effects have been the major concern of the front-end readout electronics, especially in the inner most detector region. Both single bit and multiple bits upset are observed and need to be mitigated. We propose a scheme to further study such events in irradiation tests. A parallel BER tester is built using the FPGA system where the error detector records three types of errors: single bit flip, multi-bits flip in one parallel word and multi-bits flip in two or more consecutive words. In the last type of errors, link maybe lost and need to be reestablished. Bit location, flip type, time stamp and duration of frame loss in the last type are recorded. This scheme enables longer testing duration and provides complete data logging during a SEE test for off-line data analysis. A BER bathtub curve can be scanned for link characterization. It is also the standard method for jitter extraction in Fiber Channel and Gigabit Ethernet standards. A timing delay scheme of 10ps resolution is required to acquire enough data points on the curve edge. The time-base shifting needs to be implemented before the clock recovery unit, in the analog domain. We report the bathtub scan with the clock recovery unit disabled, whose effect on link jitter can be taking into consideration through convolution using the vendor provided jitter report.

Primary author: Ms XIANG, Annie (Southern Methodist University)

Co-authors: LIU, Chonghan (Southern Methodist University); GONG, Datao (Southern Methodist University); YE, Jingbo (Southern Methodist University); DA-SHUNG, Su (Institute of Physics, Academia Sinica); HOU, Suen (Institute of Physics, Academia Sinica); PING-KUN, Teng (Institute of Physics, Academia Sinica); LIU, Tiankuan (Southern Methodist University)

Presenter: Ms XIANG, Annie (Southern Methodist University)

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