Contribution ID: **50** Type: **Poster**

The design of a low power, high speed phase locked loop

Thursday, 24 September 2009 16:55 (20 minutes)

Detector front-end readout upgrades for the ATLAS Liquid Argon Calorimeter call for radiation tolerant, high speed, and low power optical digital data links. In the development for a high speed, low power serializer ASIC, we have designed an LC-based phase locked loop (PLL) using a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS technology. Post-layout simulation indicates that we can achieve a tuning range of 4.1 –5.3 GHz with power consumption below 20 mW. The PLL will be submitted for fabrication in August, 2009. The design, optimization, and simulation results are presented.

Summary

The upgrades of the ATLAS Liquid Argon Calorimeter call for radiation tolerant, high speed, low power, optical digital data links. In the development of a 16:1 serializer for the ATLAS detector front-end readout upgrade, we have designed an LC-based phase locked loop (PLL) using a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS technology. We choose the SoS technology because of its high speed, low power, radiation tolerance, and availability of high quality analog devices like inductors. This technology has been evaluated to be suitable for development of radiation tolerant ASICs in the application of particle physics front-end readout systems. Post-layout simulation indicates that the PLL can work around 5 GHz with less than 20 mW power consumption. This PLL is a central part of a serializer working at 10 gigabit per second.

The PLL consists of a voltage control oscillator (VCO), a divider (divided by 8), a phase frequency detector (PFD), a charge pump, and a second-order low pass filter. A LC based VCO has been chosen because of its low power, high speed, and insensitivity to radiation. On-chip spiral inductors and MOSFET varactors are used as the LC tank. On-chip spiral inductors in the SoS CMOS technology have higher Q factor than those in conventional bulk CMOS silicon technologies. The varactors in the SoS CMOS technology have monotonic voltage capacitance curve and large tuning range. Six topologies of LC-based VCOs are compared and the inductors, the transistor size, the value of the current source, and the varactor size are optimized. Simulation indicates that we can achieve a tuning range from 4.1 to 5.3 GHz, a 2 V oscillation swing, a phase noise of -100 dBc/Hz at 1 MHz offset, and a power consumption less than 10 mW. The first stage of dividers is a common-current-logic (CML) divided-by-two circuit and the following two stages are CMOS. Simulation of the first stage divider indicates that the divider can work up to 5.4 GHz with less than 10 mW power consumption. The power consumption of the two CMOS dividers is very small compared with that of the CML divider. A conventional D flip-flop based PFD is implemented with dead-zone eliminated. An active unity buffer is used to minimize the charge sharing in the single-ended charge pump. We use a two-order passive low pass filter with programmable bandwidth (1.25 MHz, 2.5 MHz, and 5 MHz) to cope with different reference clock qualities

The PLL will be submitted for fabrication in August, 2009 and evaluated in the lab and in the radiation environment in the end of 2009 and in the beginning of 2010.

Primary author: Mr LIU, Tiankuan (Southern Methodist University)

Co-authors: Ms XIANG, Annie (Southern Methodist University); Mr LIU, Chonghan (Southern Methodist University); Mr SU, Da-Shung (Academia Sinica); Mr GONG, Datao (Southern Methodist University); Mr YE, Jingbo (Southern Methodist University); Mr TENG, Ping-Kun (Academia Sinica); Mr HOU, Suen (Academia Sinica); Mr LIANG, Zhihua (Southern Methodist University)

Presenter: Mr LIU, Tiankuan (Southern Methodist University)

Session Classification: POSTERS SESSION

Track Classification: ASIC's