A 16:1 serializer for data transmission at 5 Gbps

Datao Gong[1], Suen Hou[2], Zhihua Liang[1], Chonghan Liu[1], Tiankuan Liu[1], Da-Shun Su[2], Ping-Kun Teng[2], Annie C. Xiang[1], Jingbo Ye[1]

[1] Department of Physics, Southern Methodist University, Dallas TX 75275, U.S.A.

[2] Institute of Physics, Academia Sinica, Taipei 11529, Taiwan

dtgong@physics.smu.edu

Introduction

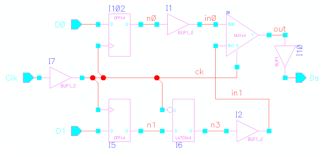
Radiation tolerant, high speed and low power serializer ASIC is used for optical link systems in particle physics. Based on a radiation tolerant commercial 0.25 μm silicon-on-sapphire CMOS technology, we designed a 16:1 serializer with a 5 Gbps serial data rate. This ASIC had been submitted for fabrication on **August 3rd 2009**. We expect to start the evaluation of this ASIC in lab and radiation environment in November 2009. All results shown here are post-layout simulation.

The serializer is implemented with robust static CMOS logic. A 2.5GHz ring oscillator based PLL is employed as a clock generator. A low power and low jitter 5GHz LC oscillator based PLL prototype for next version of serializer has been implemented on the same chip. More details about this PLL are in poster "The Design of a Low-Power, High- Speed Phase Locked Loop".

Features

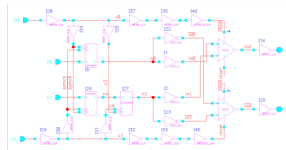
- Reference Clock 312.5MHz
- Input 16 bit LVDS data
- CML output @ 5 Gbps
- Bit error ratio < 10-12
- Single power supply of 2.5V
- Power consumption ~ 500mW
- PLL bandwidth programmable

MUX 2:1



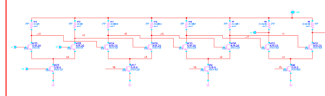
- Based on static Transmission gate D-flip-flop (DFF)
- Maximum Working Freq ~ 2GHz

High speed MUX 2:1

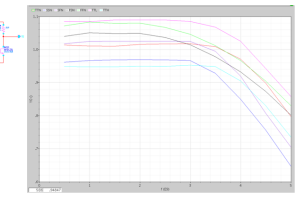


- Based on static Transmission gate DFF
- Complementary clock required
- Maximum Working Freq > 2.5GHz

CML driver



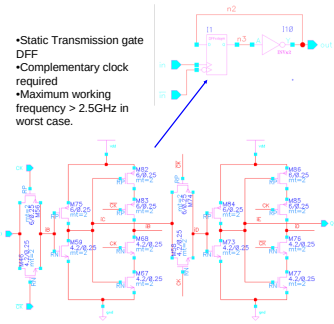
- 50 ohm termination resistors
- Current consumption ~ 100mA
- 3dB Bandwidth > 4GHz
- Peak-Peak Output amplitude > 400mV



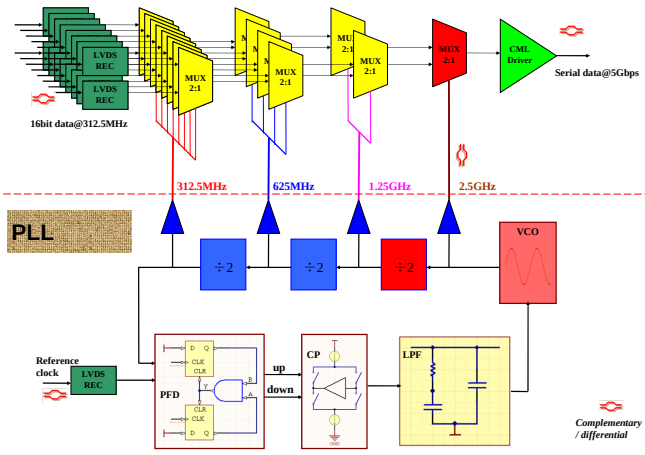
CML driver output amplitude vs input signal frequency

÷2 High speed CMOS divider

- Static Transmission gate DFF
- Complementary clock required
- Maximum working frequency > 2.5GHz in worst case.

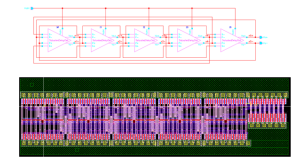


Multiplexer

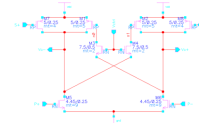


PLL

VCO



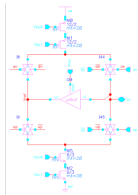
- 5 stage differential delay cell
- Two loop path to boost speed
- Area: 50 um X 200 um
- Power: 100mW Frequency: 1.5 – 2.75GHz
- Phase noise: -92 dBc@1MHz offset

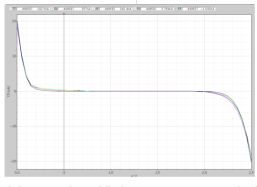


Tail current source is removed from the delay cell to eliminate the significant phase noise source. Without a current source, the oscillating amplitude is close to rail-to-rail. A consequence of this design is that the VCO is more sensitive to power noise.

Charge pump

- Charge pump current is programmable from 20 to 80uA
- Linear working range from 0.5 to 2V

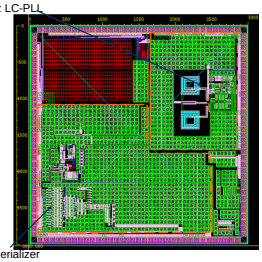




Mismatch between charge/discharge current vs control voltage

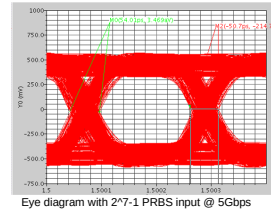
Layout of 3 mm x 3mm die

5 GHz LC-PLL



16:1 serializer

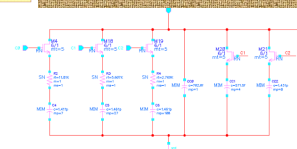
Conclusion



Eye diagram with 2^7-1 PRBS input @ 5Gbps

Deterministic Jitter (DJ) estimated from eye ~ 50 ps Random Jitter (RJ) from VCO is loop bandwidth dependant, < 2.8 ps.

Programmable LPF



LPF loop bandwidth are programmable

C0,C1,C2	001		010		100	
	bandwidth	margin	bandwidth	margin	bandwidth	margin
20uA	1.25M	60	2.5M	60	5.0M	60
40uA	2.28M	56	4.6M	56	9.1M	56
60uA	3.14M	50	6.3M	50	12.5M	50
80uA	3.88M	45	7.8M	45	15.5M	45

Acknowledgements

- This work is supported by US-ATLAS R&D program for the upgrade of the LHC, and the US Department of Energy grant DE-FG02-04ER41299.
- We would like to thank many people who have given us invaluable suggestions and comments to help us complete the design work. The incomplete name list includes Paulo Moreira (CERN), Fukun Tang (University of Chicago), Mauro Citterio, Valentino Liberali (INFN), Carla Vacchi (University of Pavia), Christine Hu, Quan Sun (IPHC), Sachin Junnarkar (BNL), Yi Kang, Jay Clementson, John Sung, and Gary Wu (Peregrine Semiconductor Corporation).
- We also would like to thank Justin Ross at Southern Methodist University for his help in setting up and maintaining the design environment.

SMU

ATLAS

twepp-09 Paris, France September 21-25, 2009