Contribution ID: **52** Type: **Poster**

Development of a 16:1 serializer for data transmission at 5 Gbps

Thursday, 24 September 2009 16:55 (20 minutes)

Radiation tolerant, high speed and low power serializer ASIC is used for optical digital data links systems in particle physics. Based on a commercial 0.25 μm silicon-on-sapphire CMOS technology, we designed a 16:1 serializer with a 5 Gbps serial data rate. We present the design details and post layout simulation results. This ASIC will be submitted for fabrication in August 2009. A shared PLL multi-channel serializer with a redundant scheme and ultra low power consumption is also discussed for applications with fibre ribbons to achieve a data throughput in tens of gigabit per second range.

Summary

A commercial 0.25 μm silicon-on-sapphire CMOS technology has been evaluated to be suitable for development of radiation tolerant ASICs for particle physics'front-end readout systems. Based on this technology we developed a 16:1 serializer with a serial data rate at 5 Gbps. The serializing unit consists of a cascade of 2:1 multiplexing circuit based on a static D-flip-flop for its better SEE immunity. In this design only the last 2:1 multiplexing stage works at 5 Gbps or the highest speed. This provides the possibility of using dynamic circuit with majority voting in future designs for speeds above the static D-flip-flop. A simple divide-by-two divider chain is used in the clock system and this greatly simplifies the design especially at high speed. A differential ring oscillator based PLL provides the 2.5 GHz clock with 50% duty cycle, generated from the 312.5 MHz reference clock. The PLL loop bandwidth is programmable to cope with different reference clock qualities. In order to check the overall behavior of this PLL, a c++ based behavior model and a jitter analysis tool have been developed. A CML driver is developed for the electric output signal. Post layout simulation provides power consumptions for each function block to be 45 mW for LVDS receiver, 135 mW for the PLL, 102 mW for the serializing unit and 82 mW for the CML driver. The total power consumption is less than 400 mW, or 80 mW/Gbps.

In order to achieve data throughout in 25 Gbps range, for applications in the ATLAS liquid argon calorimeter front-end readout upgrade, we designed a 5-in-6-out serializer ASIC with a shared PLL and a redundancy scheme, for optical links with a 12-way fibre ribbon (two serializer chips and a total throughput about 50 Gbps). The redundancy improves system reliability, an issue in applications in particle physics where the front-end electronics are usually inaccessible for maintenance. The power consumption is estimated to be 1.5 W or 50 mW/Gbps. This idea will also be implemented in future designs based on a faster LC based PLL to boost the data throughput into 40-50 Gbps range to achieve a throughput of 80-100 Gbps with one 12-way fibre ribbon.

This design will be submitted in August 2009. We will evaluate this ASIC in lab and in radiation environment starting in the winter of 2009 and 2010.

Primary author: Mr GONG, Datao (Southern Methodist Univeristy)

Co-authors: Ms XIANG, Annie (Southern Methodist Univeristy); Mr LIU, Chonghan (Southern Methodist Univeristy); Mr SU, Da-Shung (Institute of Physics, Academia Sinica); Prof. YE, Jingbo (Southern Methodist Univeristy); Mr TENG, Ping-Kun (Institute of Physics, Academia Sinica); Mr HOU, Suen (Institute of Physics, Academia Sinica); Mr LIU, Tiankuan (Southern Methodist Univeristy); Mr LIANG, Zhihua (Southern Methodist Univeristy)

Presenter: Mr GONG, Datao (Southern Methodist Univeristy)

Session Classification: POSTERS SESSION

Track Classification: ASIC's