IN2P3

Omega

LAL

PARISROC
Photomultiplier ARray Integrated in Sige Read Out Chip

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AGENCE NATIONALE DE LA RECHERCHE
ANR

PMm²

Orsay MicroElectronics Group Associated

Contents

- PMm² project
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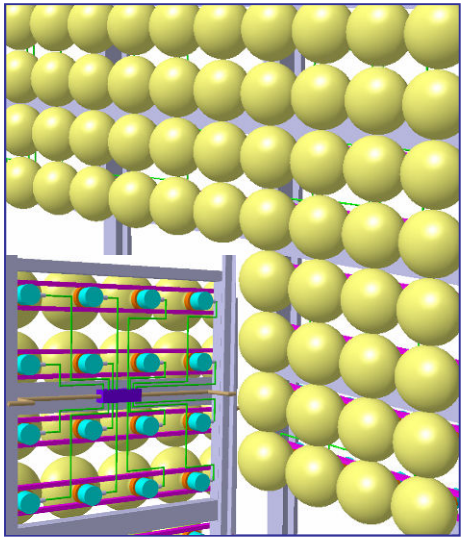
- Measurements
- Conclusion



AGENCE NATIONALE DE LA RECHERCHE
ANR

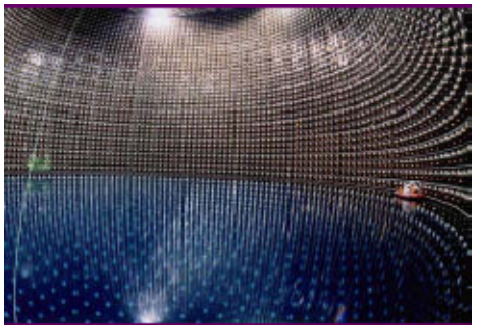
PMm²

PMm² Project (I)

- ***PMm² : Innovative electronics for array of photodetectors used in High Energy Physics and Astroparticles.***

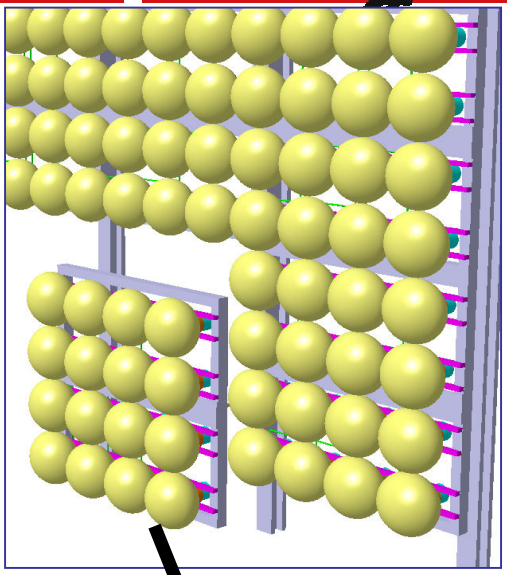
- **R&D program funded by French national agency for research (ref. ANR-06-BLAN-0186) (LAL, IPNO, LAPP , ULB Bruxells and Photonis) (2007-2010)**

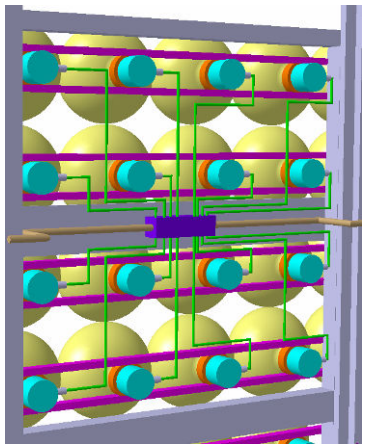
- **Application : large water Cerenkov neutrino detectors (more generally: exp. with large number of PMTs)**



PMm² Project (II)

- The project proposes to segment the very large surface of photodetection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics.
- Replace large PMTs (20 inch) by groups of 16 smaller ones (12 inch) with central ASIC :
  - Independent channels
  - charge and time measurement
  - water-tight, common High Voltage
  - Only one wire out (DATA + VCC)
- Target :
  - 1pe efficiency
  - Triggerless acquisition
  - 1ns time resolution
  - High granularity
  - scalability
  - **Low cost:**

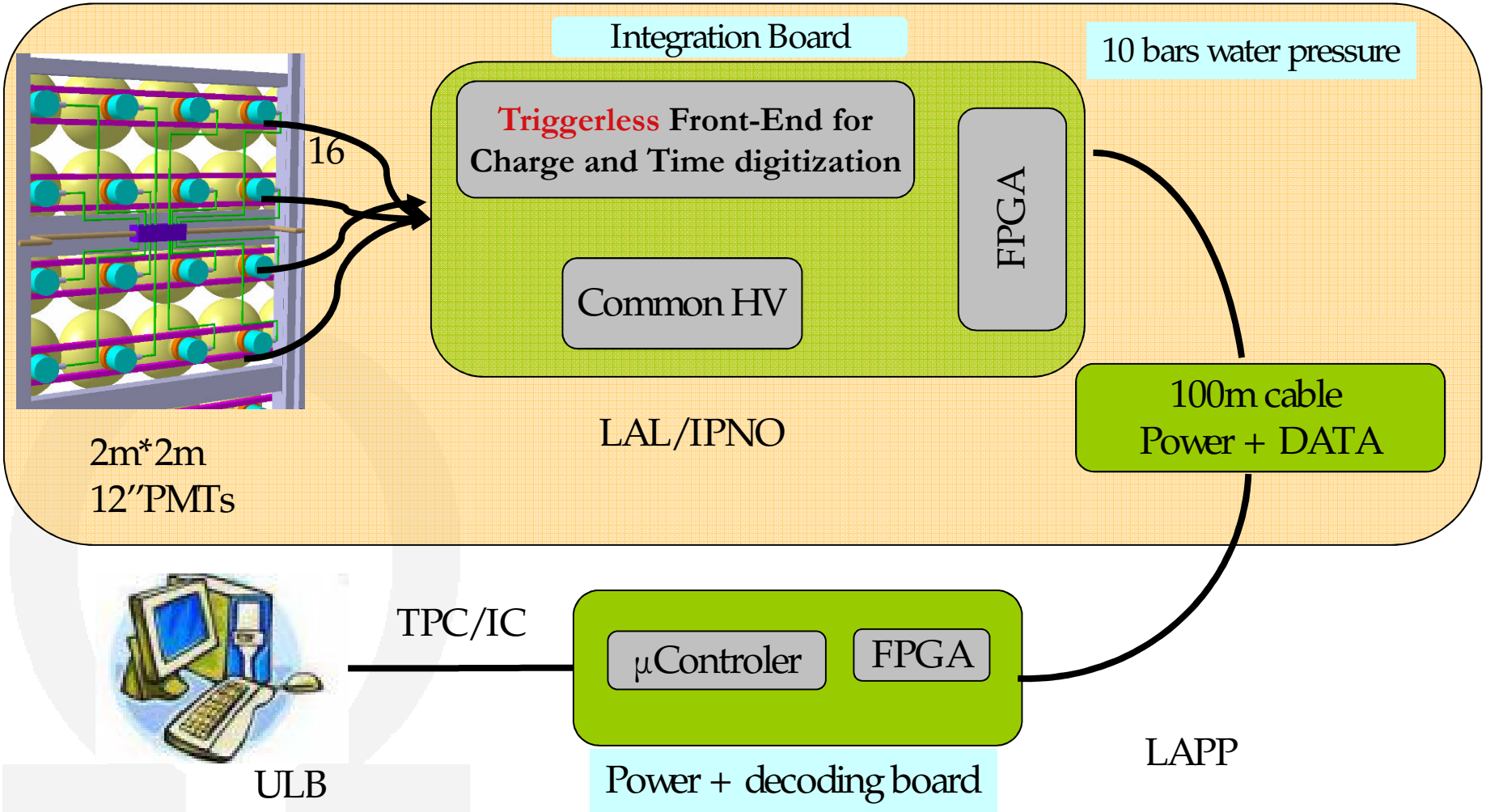




- Common HV for 16 PMTs
- Common electronics for 16 PMTs
- Front-end closed to the PMTs array

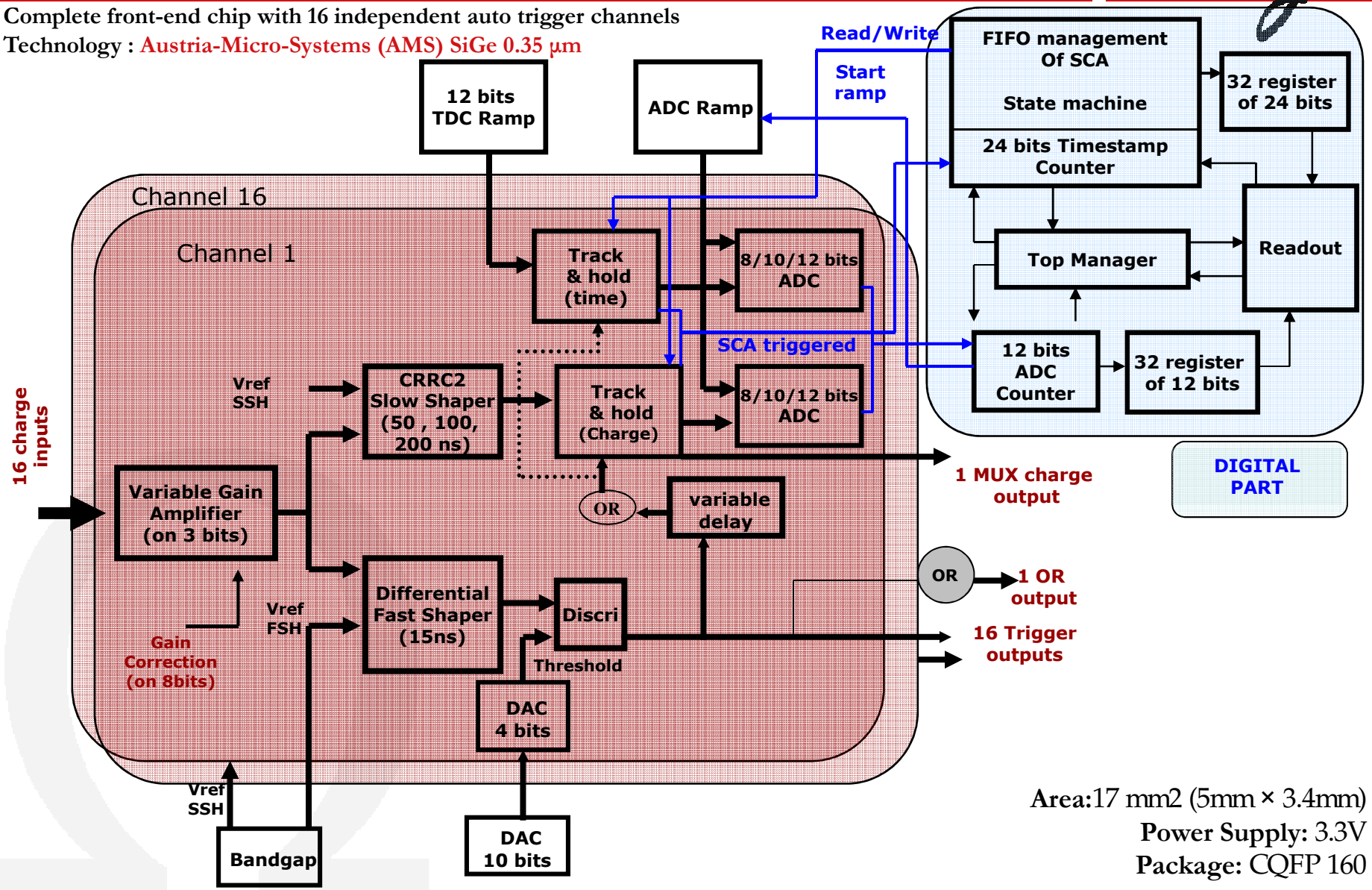
PMm² Project (III)

The general principle of PMm² project is that the ASIC and a FPGA manage the dialog between the PMTs and the surface controller



PARISROC architecture

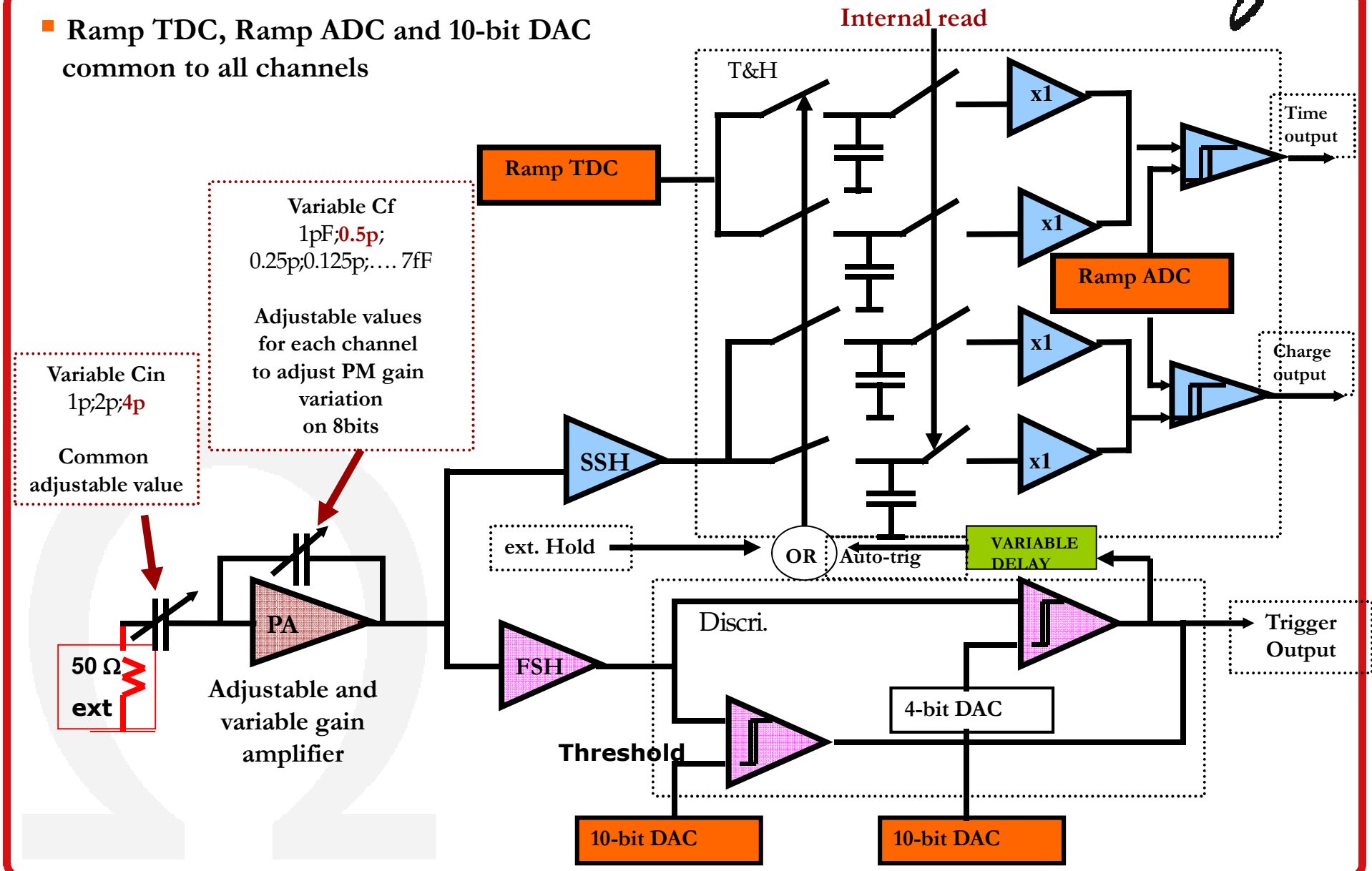
Complete front-end chip with 16 independent auto trigger channels
Technology : Austria-Micro-Systems (AMS) SiGe 0.35 µm



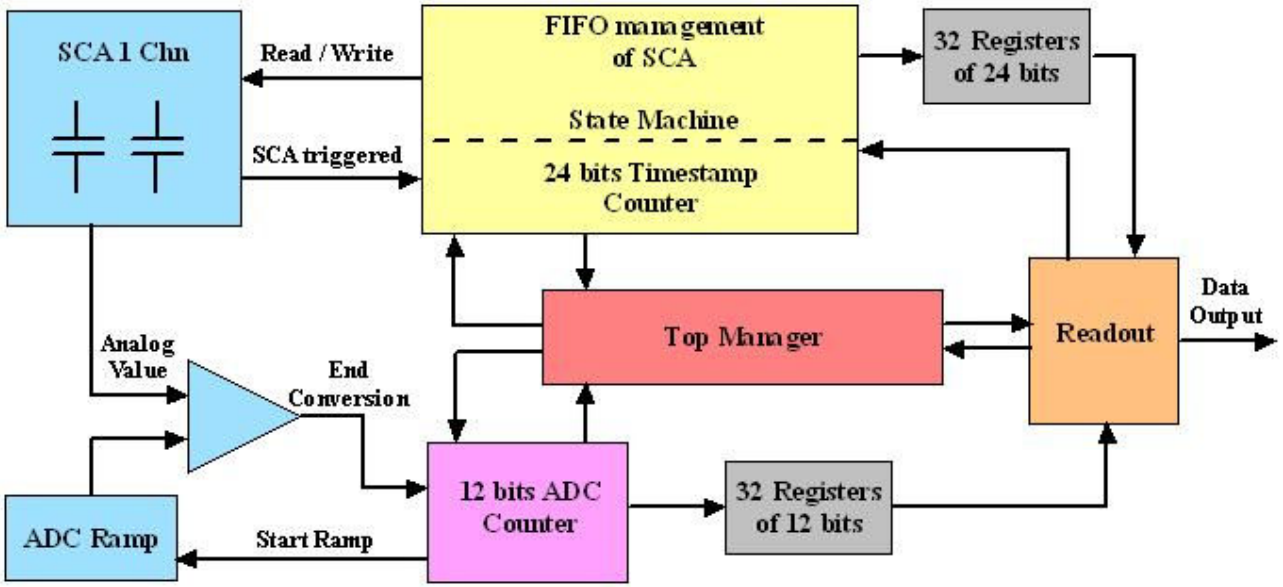
Area:17 mm2 (5mm × 3.4mm)
Power Supply: 3.3V
Package: CQFP 160

One channel analog part

- Ramp TDC, Ramp ADC and 10-bit DAC common to all channels



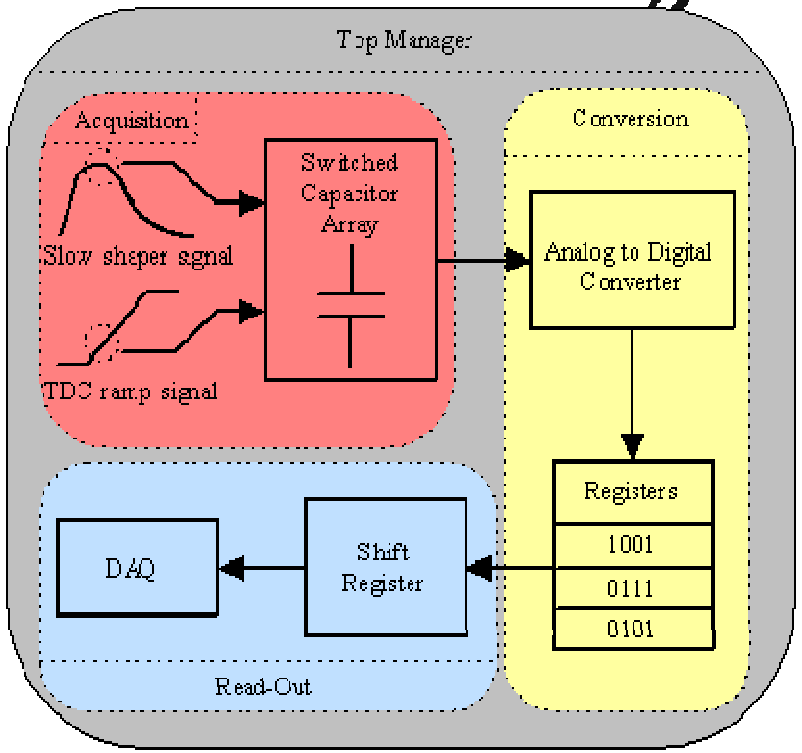
Digital part architecture(I)



- 16 channels managed independently
- 2 state machine dedicated to handle one channel: Write and Read
- SCA depth of 2 for time and charge measurement
- SCA management like FIFO
- 24bits Timestamp counter @ 10 MHz (1.67s)
- 32 registers of 24 bits to save coarse time for each depth of SCA
- 32 registers of 12 bits to store converted data: 16 charge and 16 fine time
- 40 MHz clock for ADC + SCA management
- 10 MHz clock for Timestamp + Readout

Digital part architecture(II)

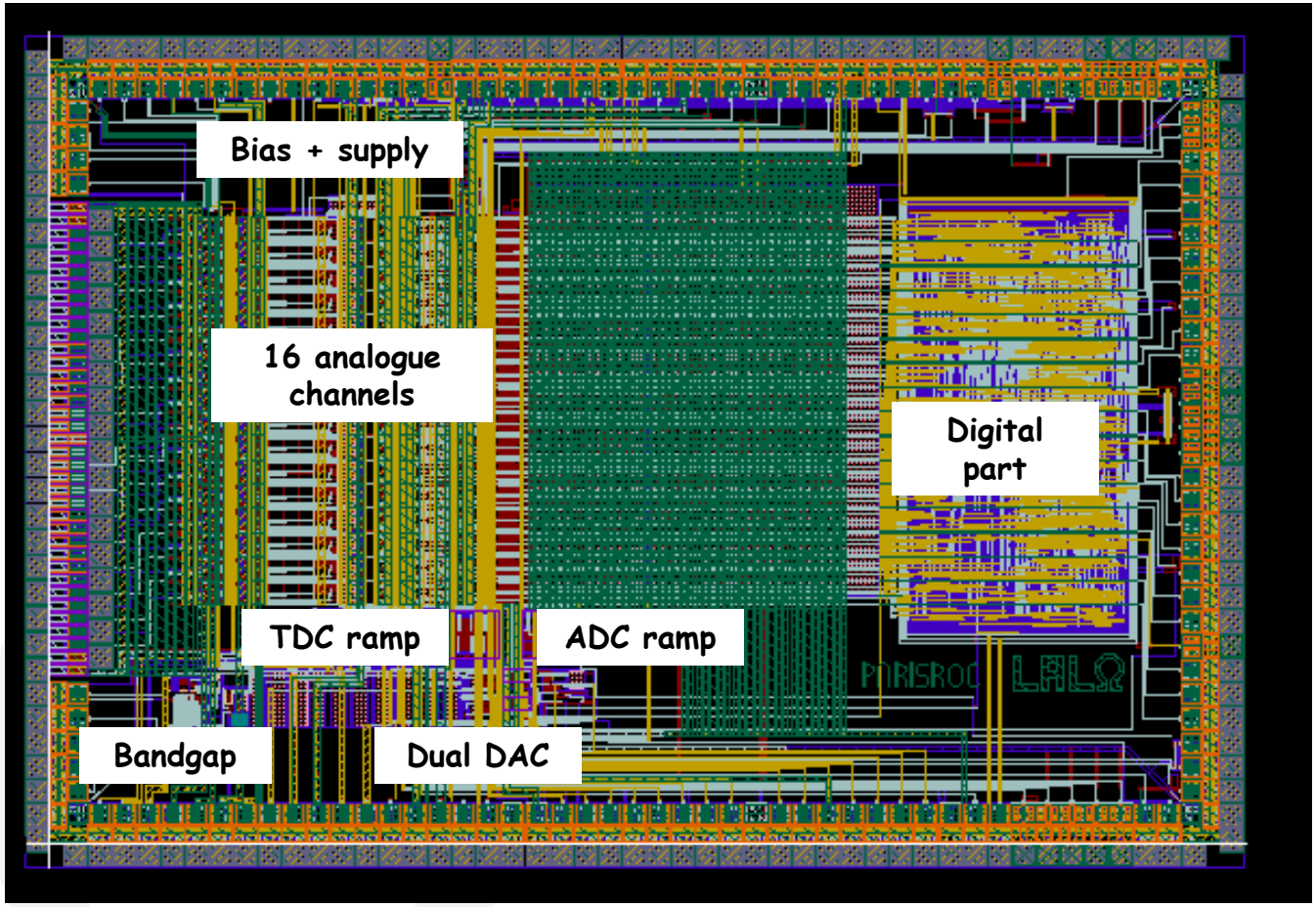
- 4 modules: *Acquisition, Conversion, Read Out and Top manager.*
- Acquisition: Analog memory
- Conversion: Analog charge and time into 12 bits digital value saved in register (RAM)
- Read Out: RAM read out to an external system



Selective Read Out

- Only hit channels are readout
- Readout clock : 10 MHz
- Max Readout time (16 ch hit) : 100 us
- 52 bits of data / hit channel (all gray)
- Readout format (MSB first) : 4 bits channel # +
  24 bits timestamp +
  12 bits charge +
  12 bits time

PARISROC layout



Technology :

AMS SiGe 0.35mm

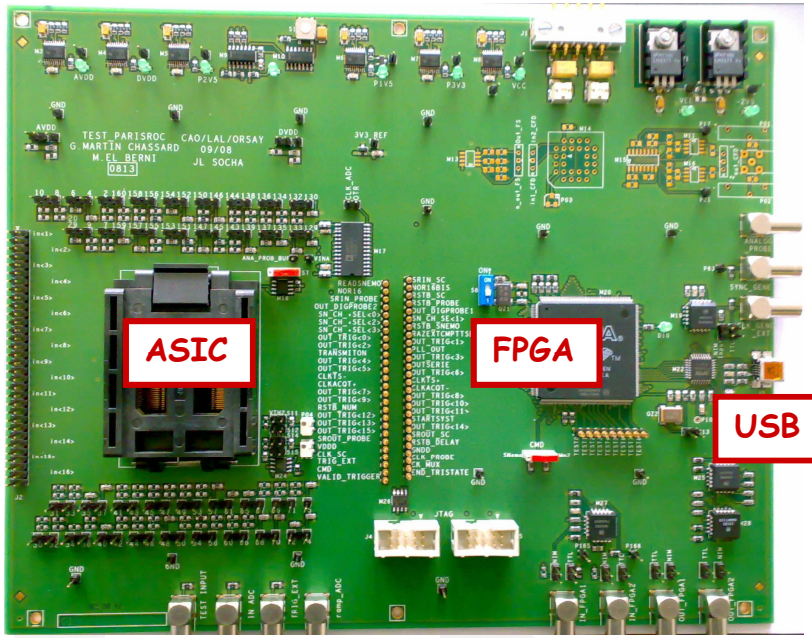
Size : 5mmX3.4mm

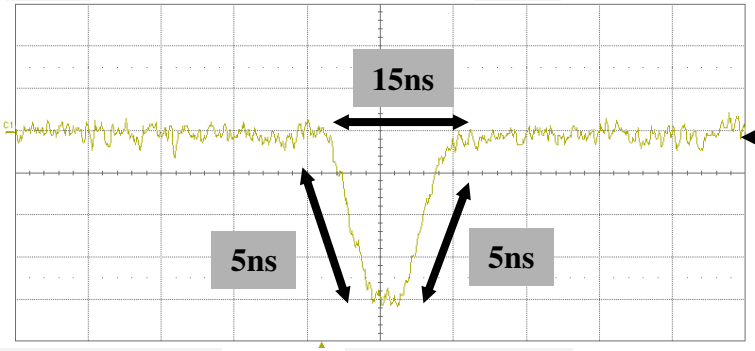
Package :

CQFP160

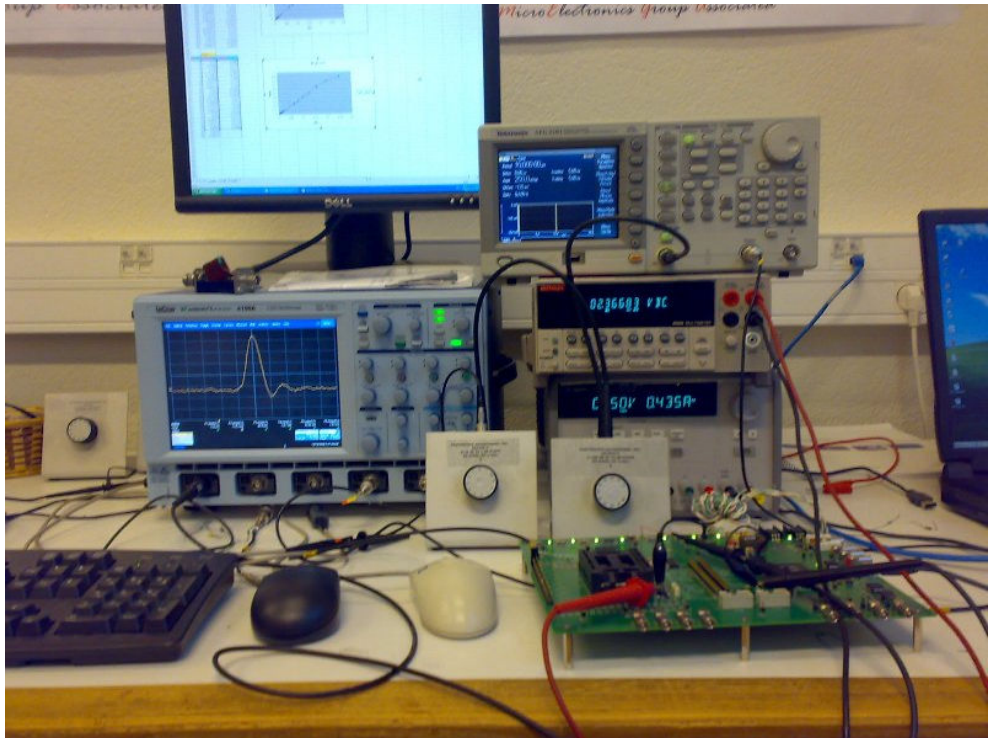
Measurements

TEST BOARD





TEST BENCH

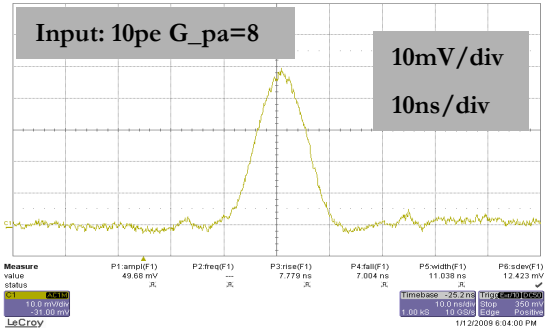


input signal : *Ii= 0 to 5mA*
0 to 300 pe → 0 to 50 pC
PM's Gain=10⁶ (1pe=160 fC)

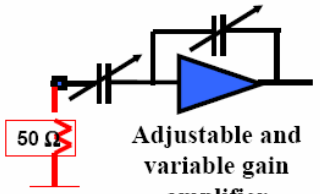
PARISROC submitted in June 08 and received in December 08

Analog measurements: Preamplifier

1.Preamplifier	Meas.	Sim
RMS NOISE without USB cable	1mV 660uV	468uV
Noise in pe without USB cable	0.2 0.132	0.086
Vout(1pe)(G_pa=8)	5mV	5.43mV
SNR without USB cable	5 7.6	11.6



High speed : tr=5ns

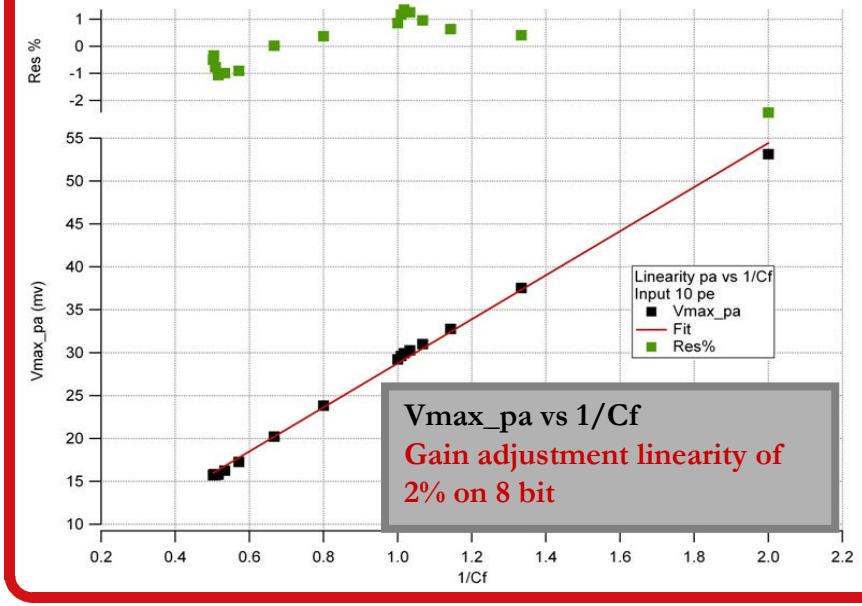


Gain uniformity for all channels (Vmax_pa vs Channels; CF var; Cin=4pF); 100 pe input.

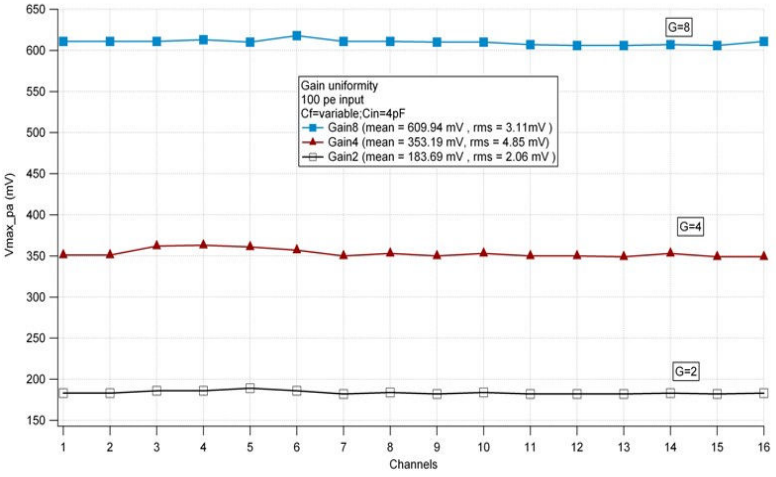
PA_GAIN	Mean(mV)	Rms(%)
8	609.94	0.5
4	353.19	1.4
2	183.69	1.2

Linearity pa for 10 pe input signal

Residuals in %	-2.5 <Res% <1.35



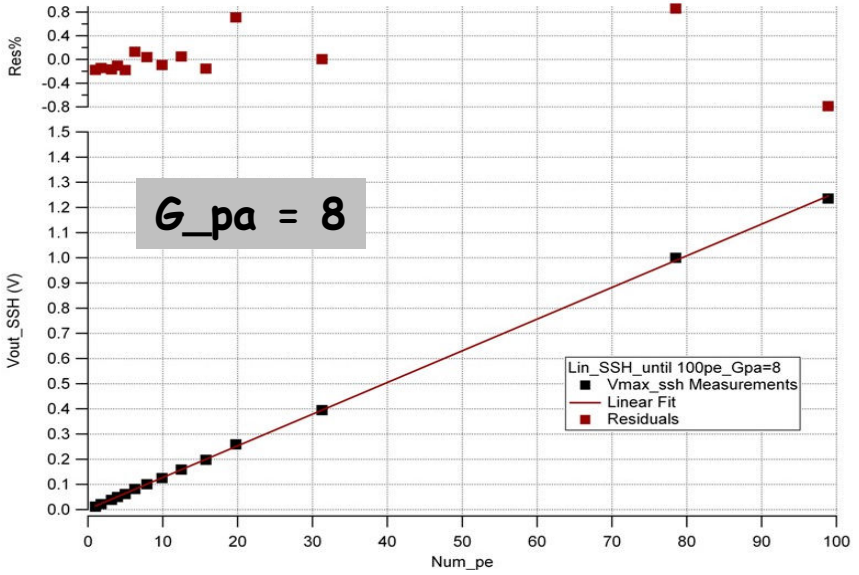
Vmax_pa vs 1/Cf
Gain adjustment linearity of 2% on 8 bit



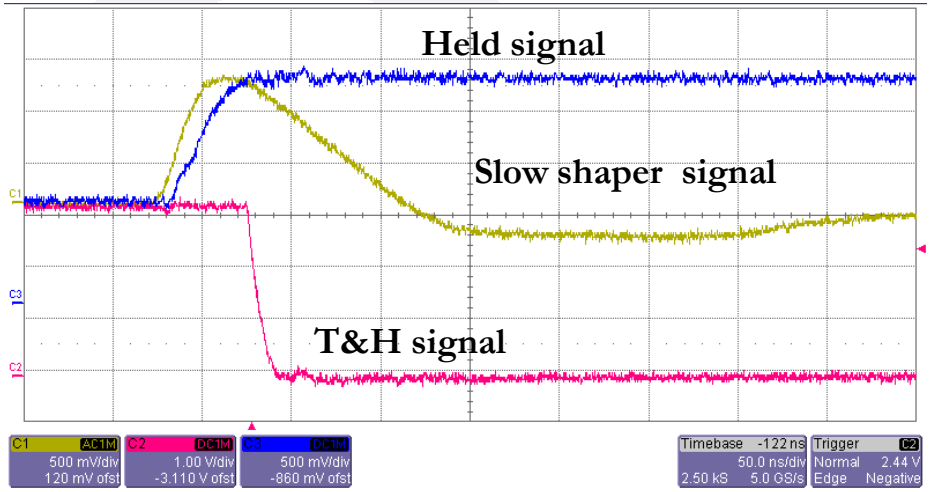
Slow Shaper

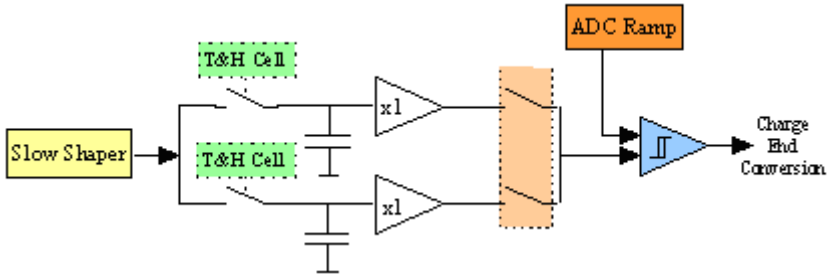
1. Slow shaper (50ns)	Meas.	Sim
RMS NOISE	4mV	2.3mV
Noise in pe	0.3	0.125
Vout(1pe)(G_pa=8)	12mV	19mV
SNR	3	8

Extra noise sources:
- 10 MHz Clock : doubles the noise
- Low frequency noise



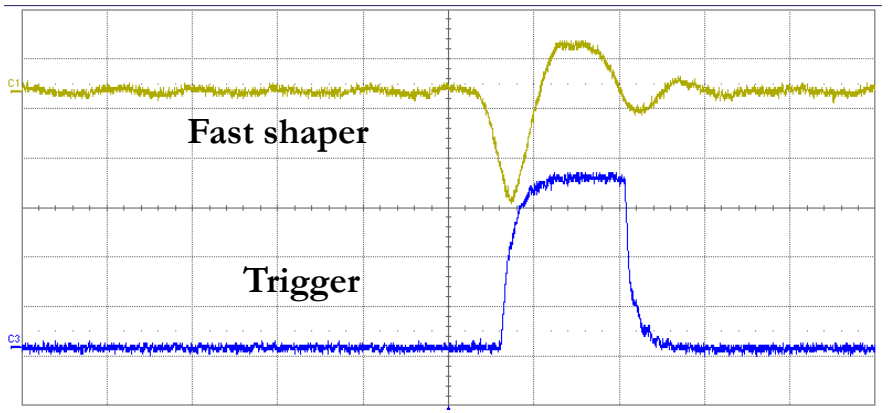
SSH Linearity better then 1% at high preamplifier gain.



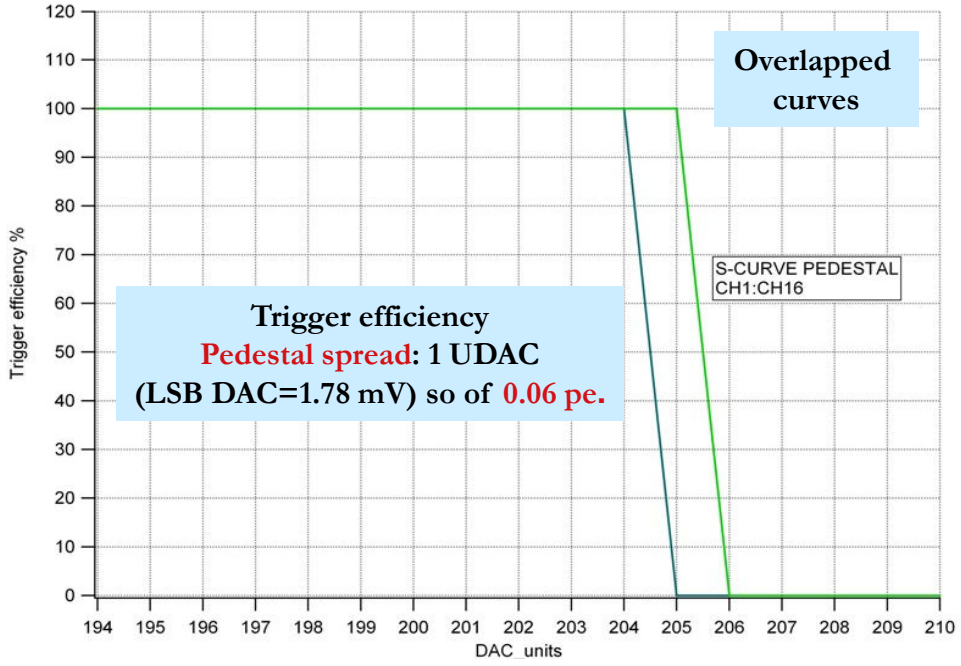


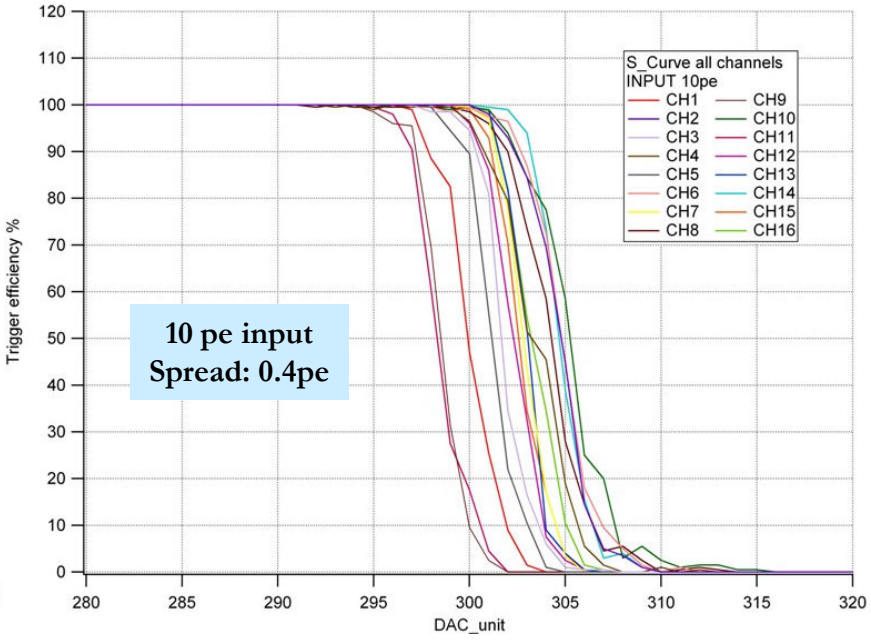
Fast shaper and discriminator

3. Fast shaper (G_pa=8)	Meas.	Sim
RMS NOISE	2.5mV	2.36mV
Noise in pe	0.08	0.06
Vout(1pe)(Gpa=8)	30mV	39mV
SNR	12	16



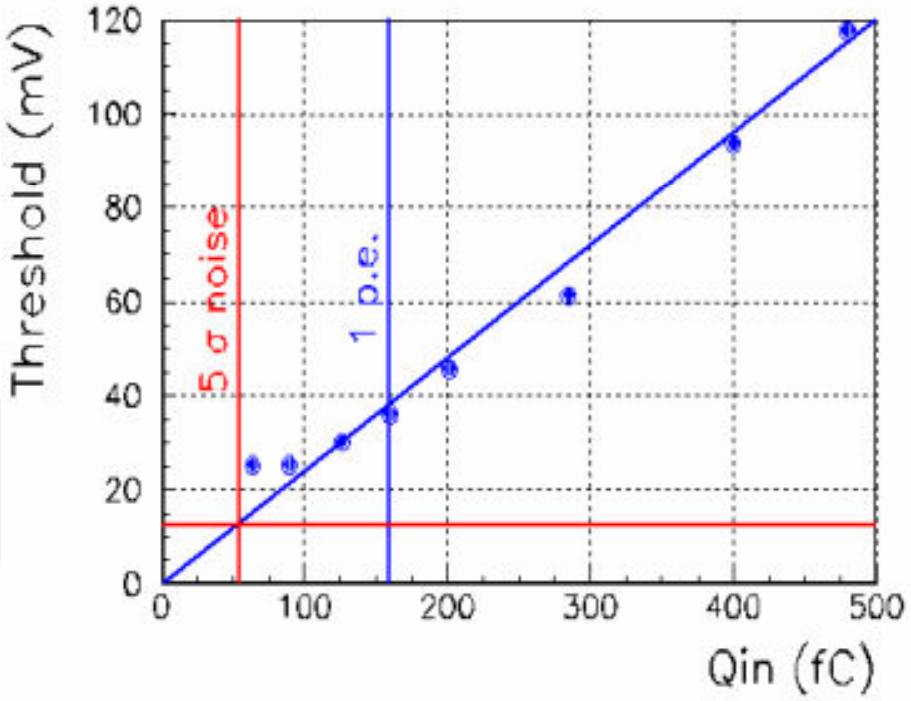
Pedestal spread better than 0.1 pe.

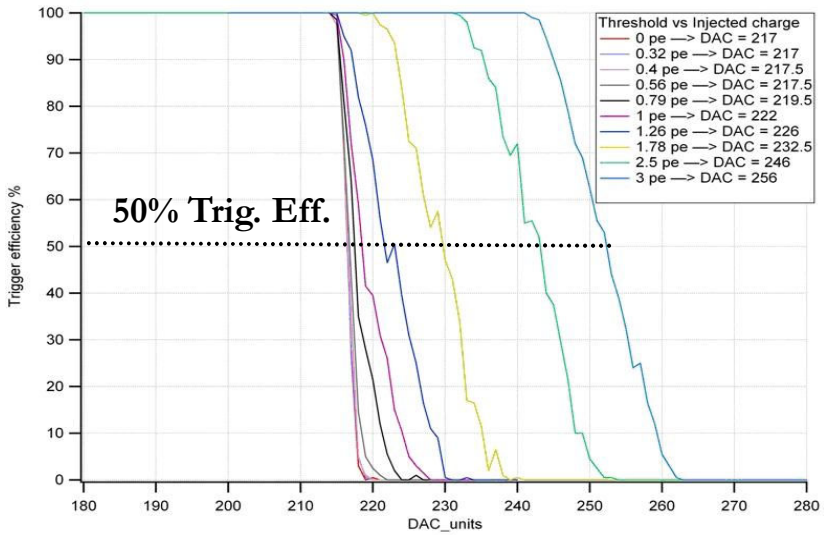


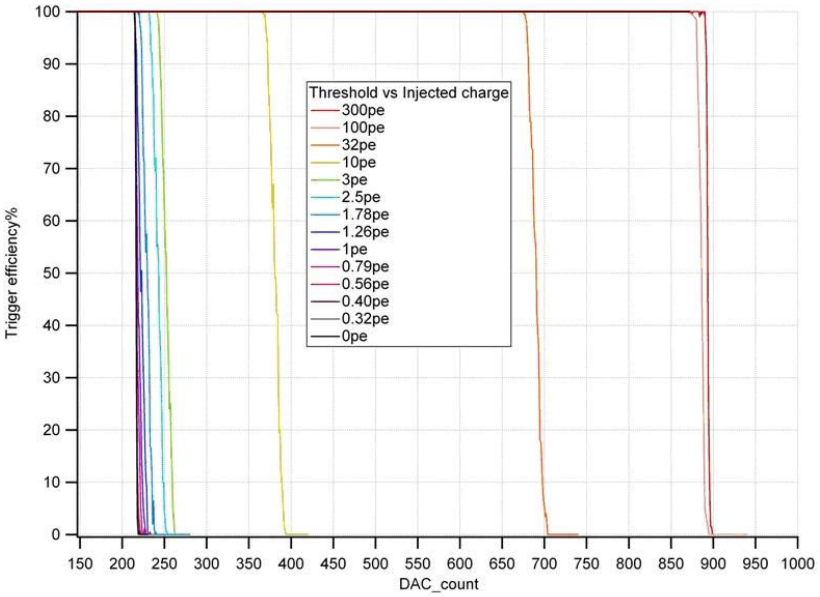


Trigger efficiency

- Trigger down to 100 fC and up to 5pC
- Noise 10 fC
- Limited to 10 σ due to discriminator coupling





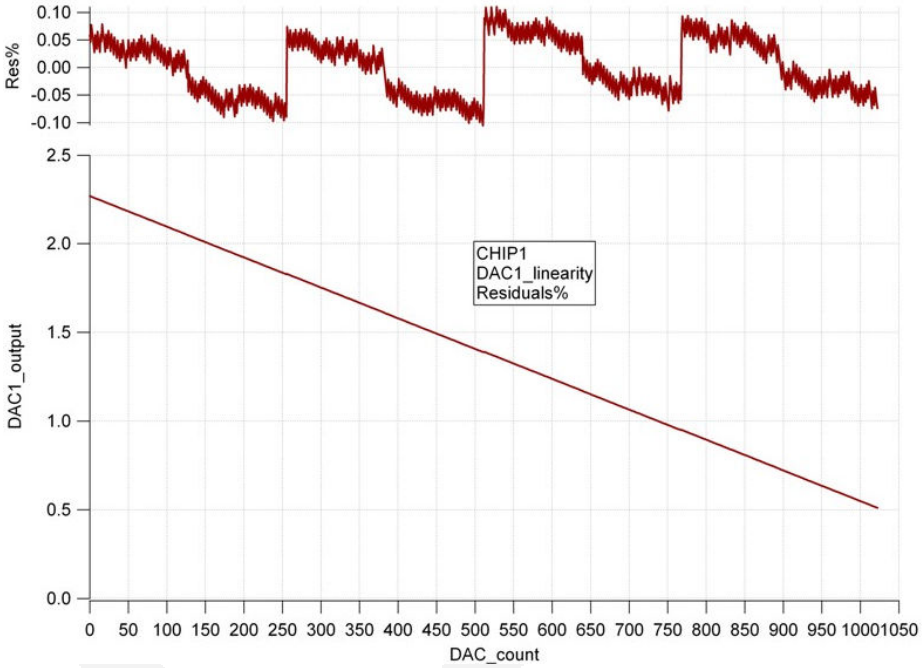


10 bit DAC Linearity

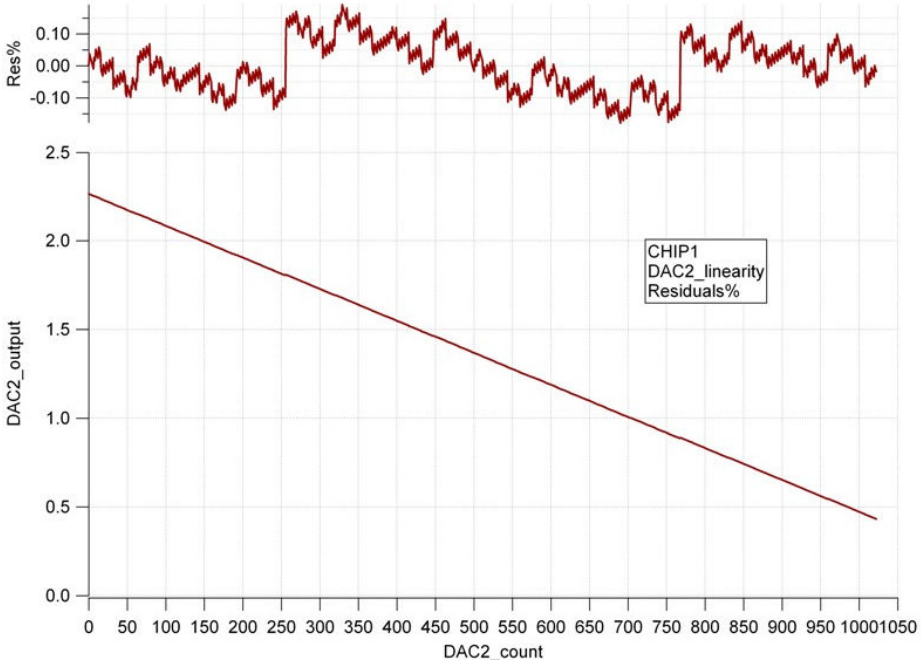
	Residuals(%)
DAC1_Chip1	-0.1 to 0.1
DAC2_Chip1	-0.1 to 0.1

Linearity at 0.1%

DAC1_LINEARITY_CHIP1



DAC2_LINEARITY_CHIP1



Internal Wilkinson ADC (I)

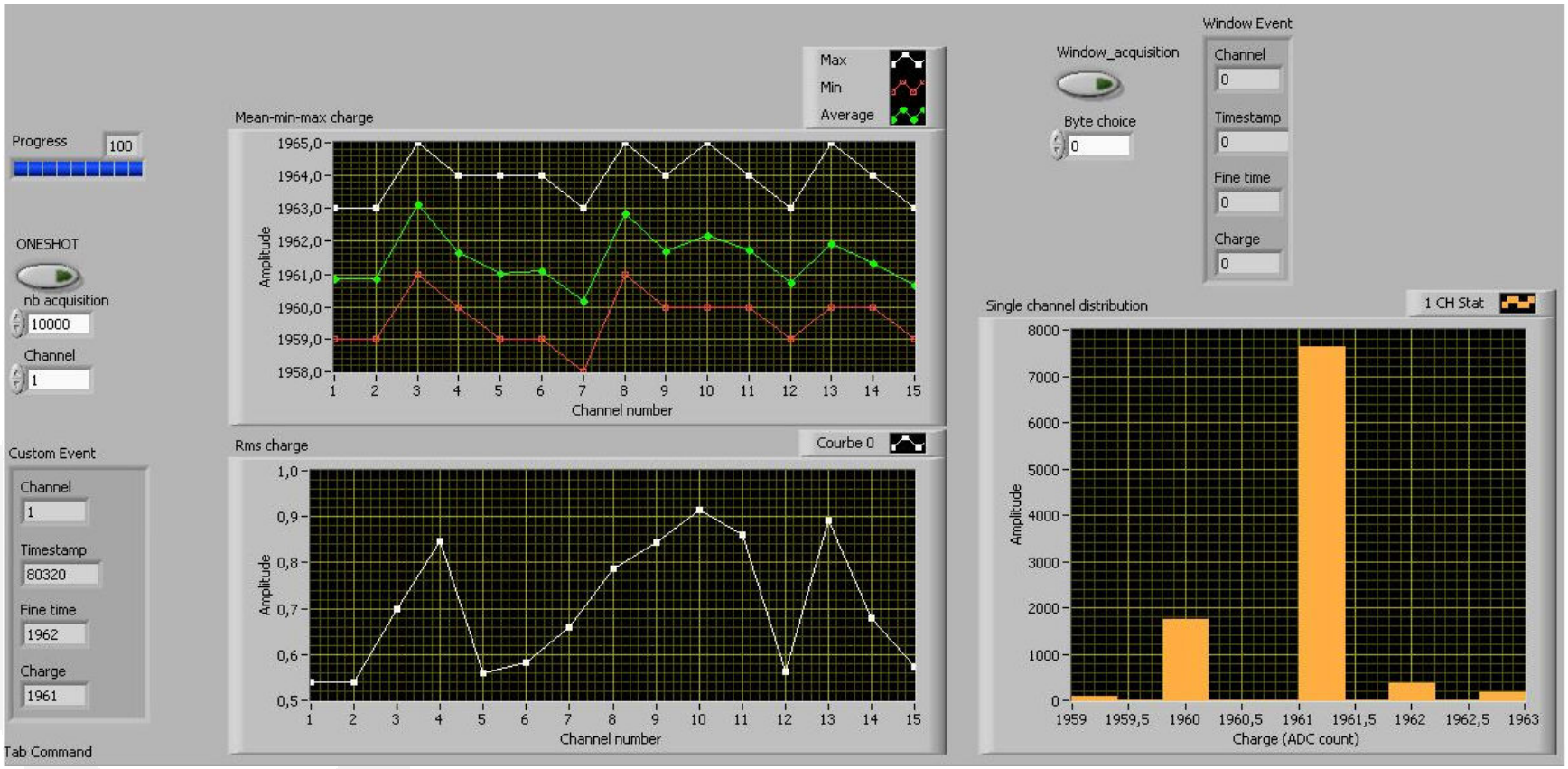
DAC=500=1.4523V

Number of acquisitions: 10000

12 bit ADC (LSB=269μV)

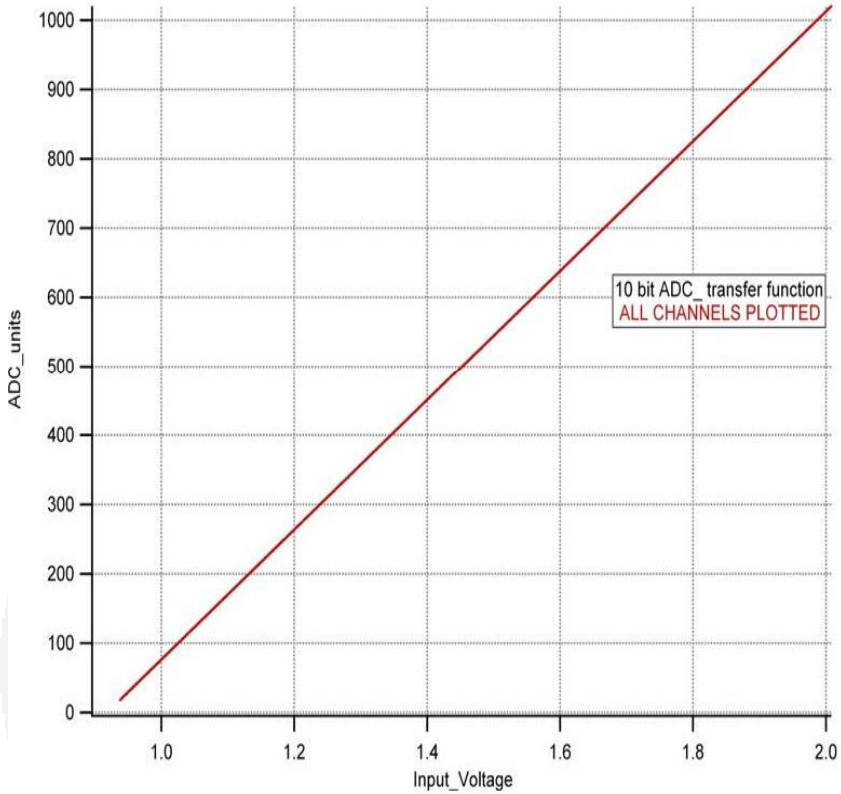
ADC_UNITS=1961

ΔADC_units=5

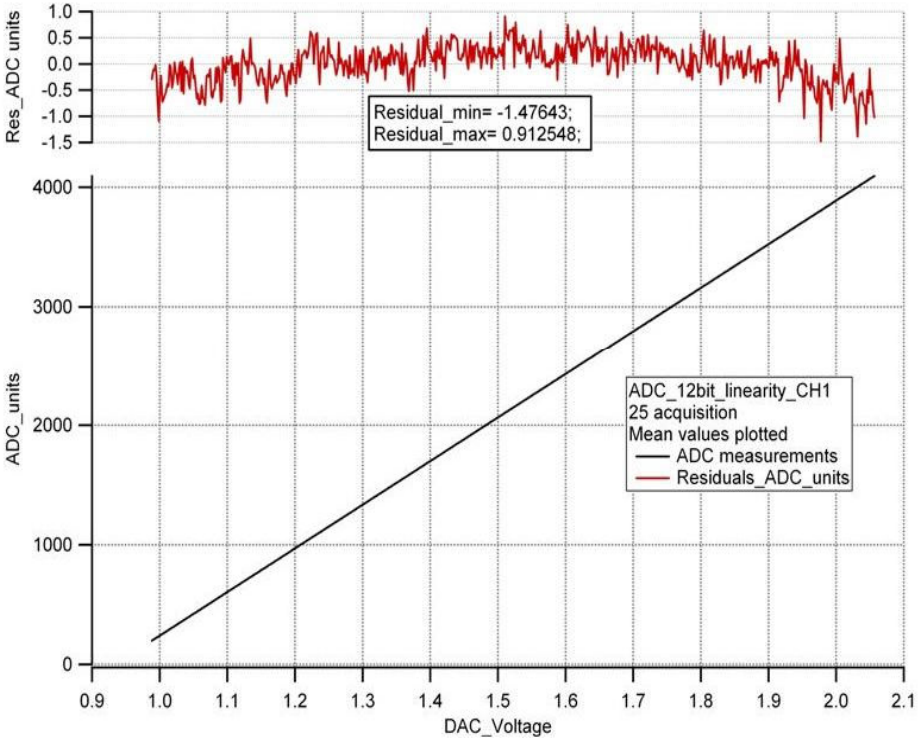


Internal Wilkinson ADC (II)

- The ADC is suited to a multichannel conversion
- Very good uniformity and linearity



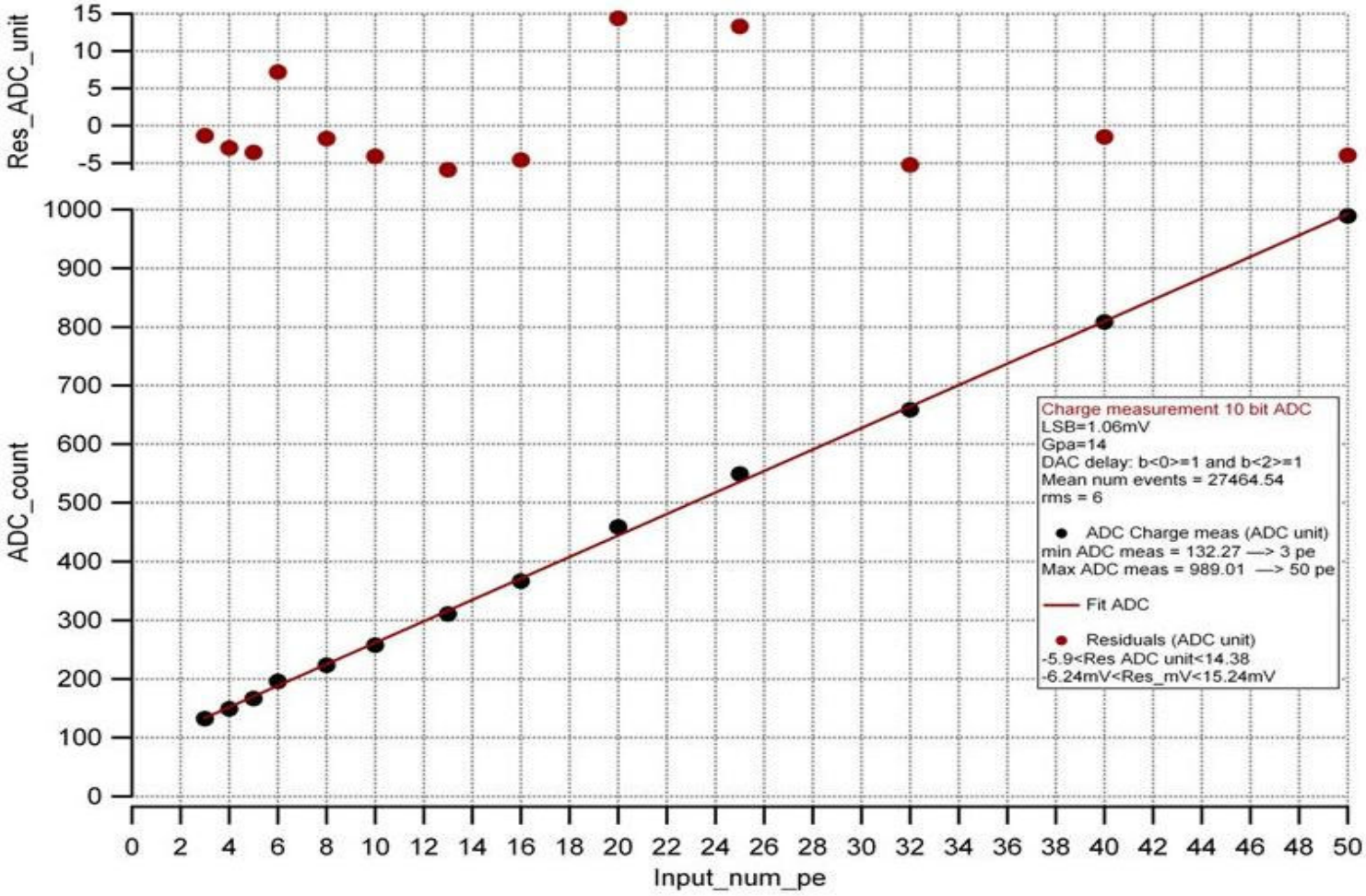
Uniformity of 10 bit Wilkinson ADC
16 channels superimposed!



Linearity at 1%
of 12 bit Wilkinson ADC

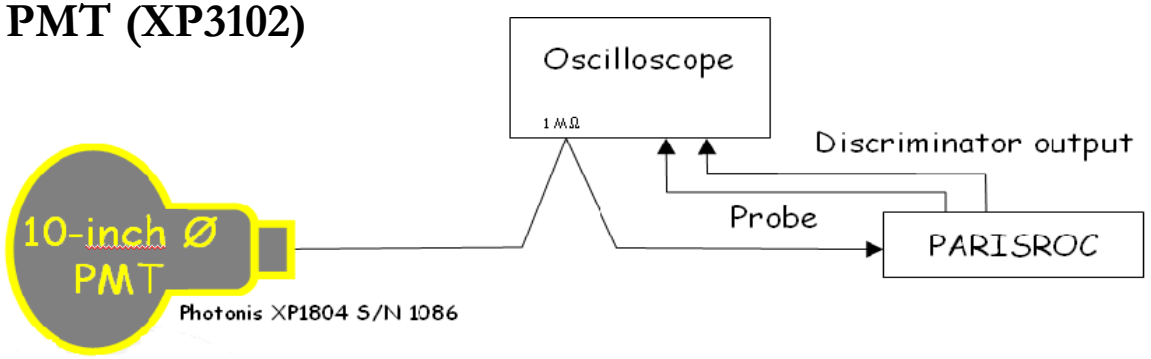
Overall behavior (10 bit ADC)

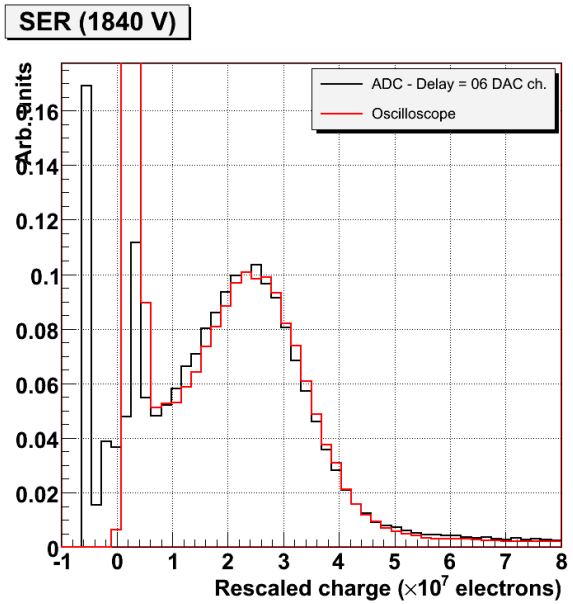
- Complete chain: Autotrigger + T&H + Internal ADC
- Linearity : 1% ; Noise 6 UADC (10 bit LSB=1.06mV)

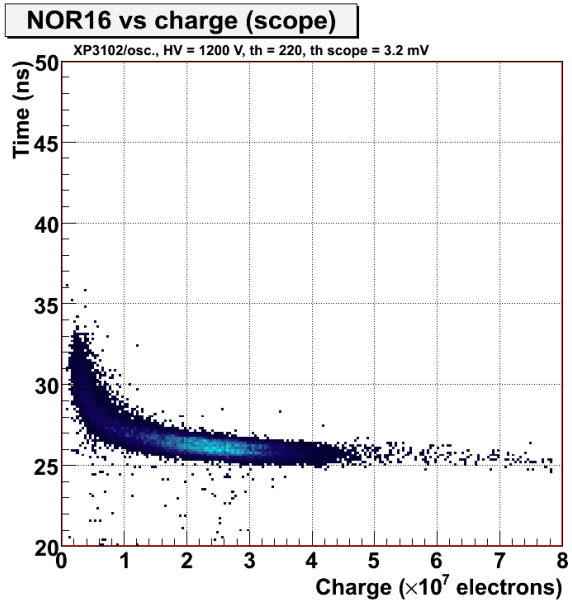


Measurement with PMT [B.Genolini IPNO]

- **SPE spectrum with 10 inch PMT X**
  - Complete chain : outotrigger + 10 bit internal ADC
- **Time measurement with 2 inch PMT (XP3102)**
  - Trigger output jitter : 600 ps







Conclusion and next steps

- **Good Overall performance of PARISROC.**

- Autotrigger and internal digitization;
- Very good uniformity and linearity;
- Extra noise source :
  10 MHz Clock double the noise,
  Low frequency noise.

- **A second version will be done in November 09.**

- Possible PMT gain increasing ;
- Increase dynamic range with 2 gain ;
- 8, 9, 10 bit ADC to reduce dead time ;
- Double fine TAC.

- **Chip being evaluated by several experiments:**
  Memphys, DUSSEL, LENA……..

BACKUP

Costs

Size (Diameter)	20	20(17)	12	Inch
Photocathode area	1660	1450	615	cm^2
Quantum efficiency	20	20	24	%
Collection efficiency	60	60	70	%
Cost	2500	2500	800	€
	12.6	14.4	7.7	€ /PE_U/cm^2

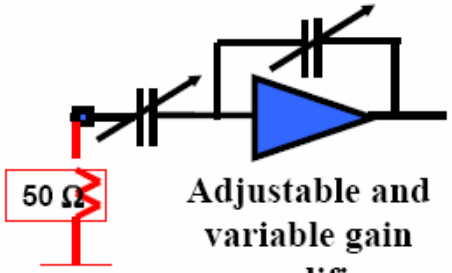
Cost/cm^2 per useful photoelectron

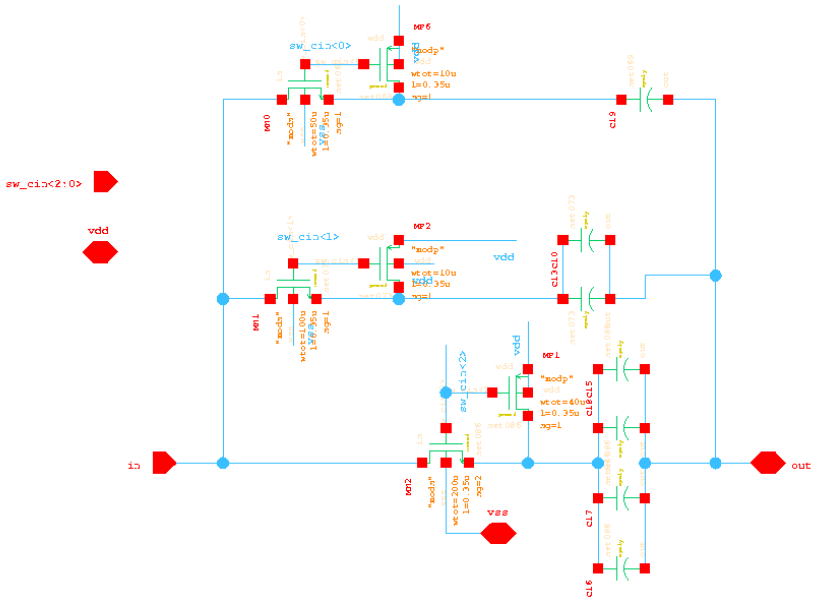
Cost / (cm^2 x QE x CE)

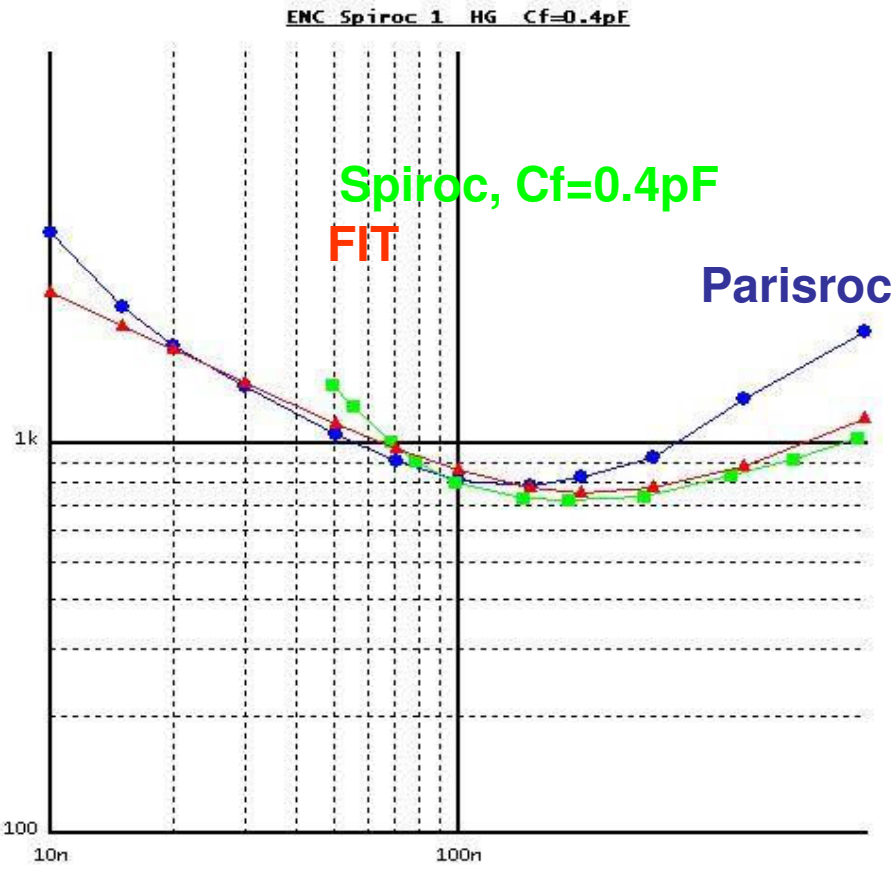
12" is better in SER and timing

12" provides a higher granularity

But, the number of channels is increased


50 Ω
Adjustable and
variable gain
amplifier




ENC Spiroc 1 HG Cf=0.4pF
Spiroc, Cf=0.4pF
FIT
Parisroc
1k
100
10n
100n

Clock Noise

Channel 9

Without Clock	With 40 MHz Clock	With 10 MHz and 40 MHz Clock
Rms noise ssh 2.6mV	Rms noise ssh 3mV	Rms noise ssh 5mV

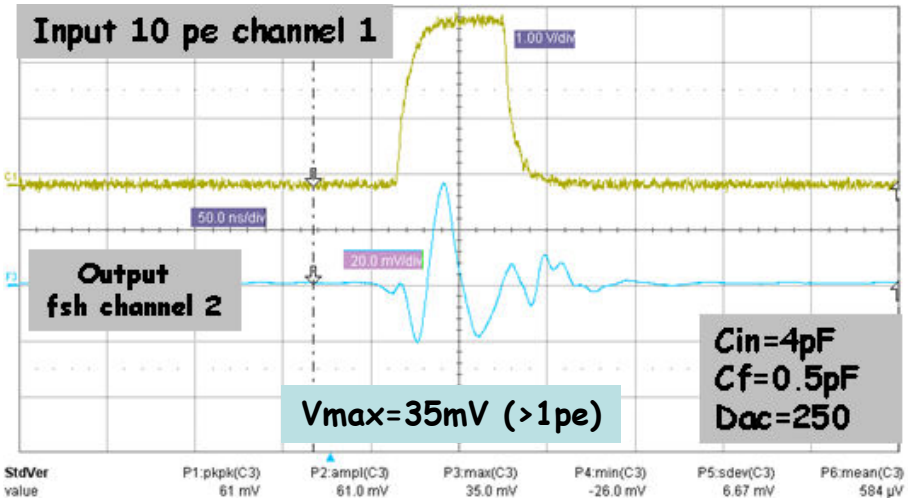
Channel 1

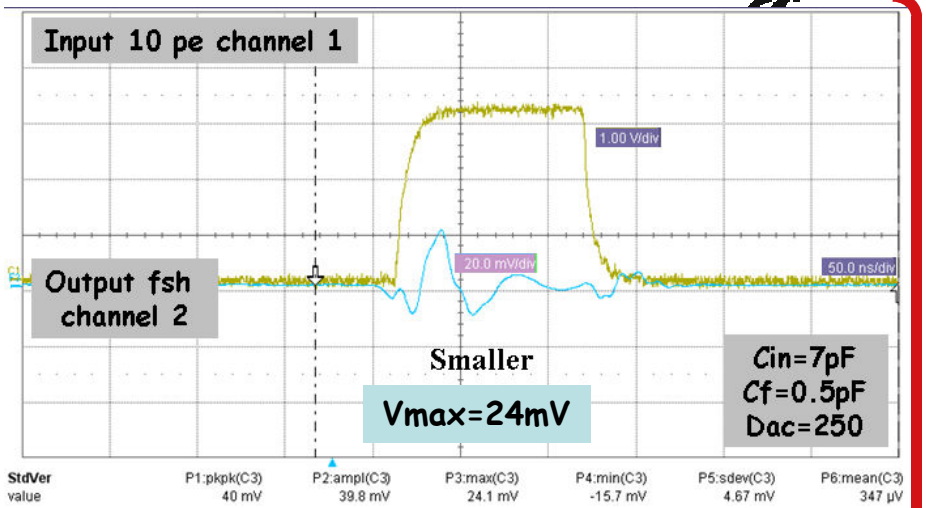
With 10 MHz and 40 MHz Clock
Rms noise ssh 10mV

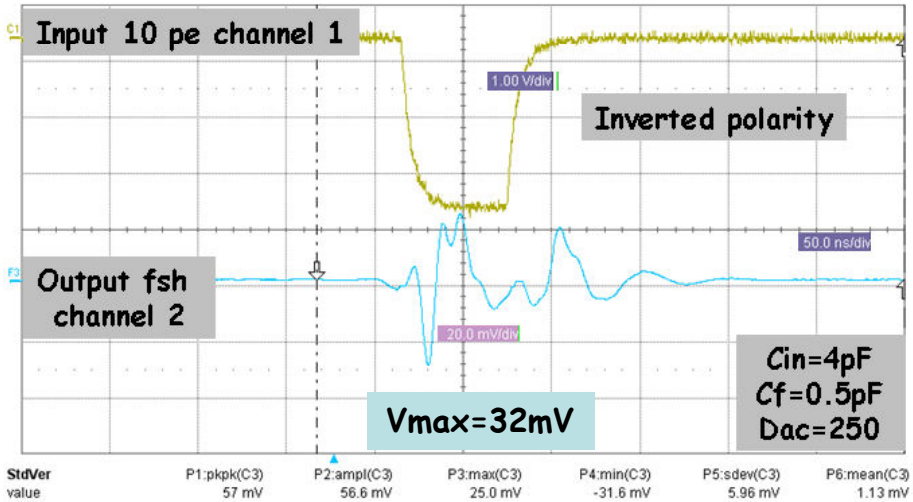
0.4 mV of noise due to 40MHz Clock
And 2mV noise due to 10MHz Clock

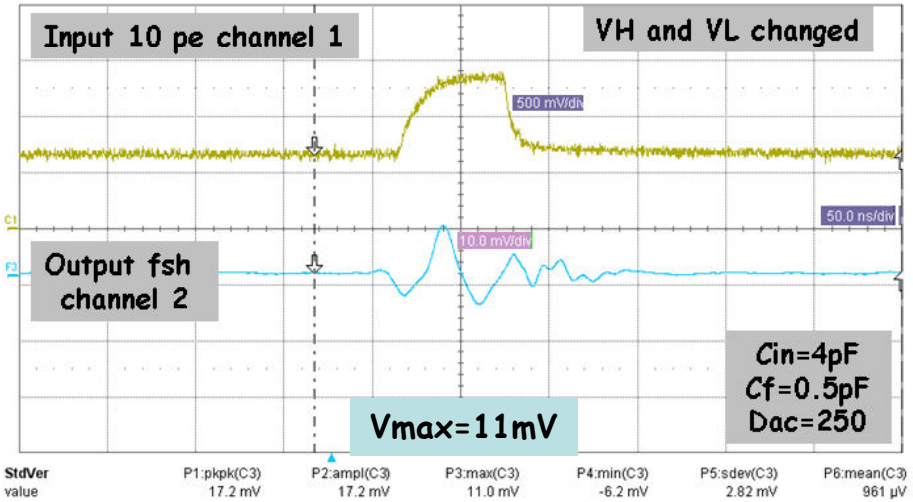
- Rms noise is bigger with Clocks in particular with 10MHz Clock
- Clk noise is progressively smaller from Channel 1 to Channel 16
- Clk noise is smaller with smaller preamplifier gains

Discriminator coupling

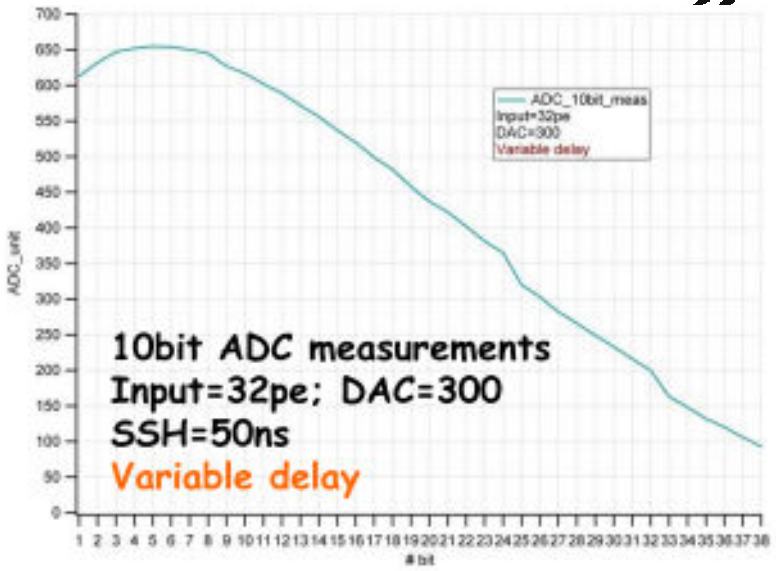


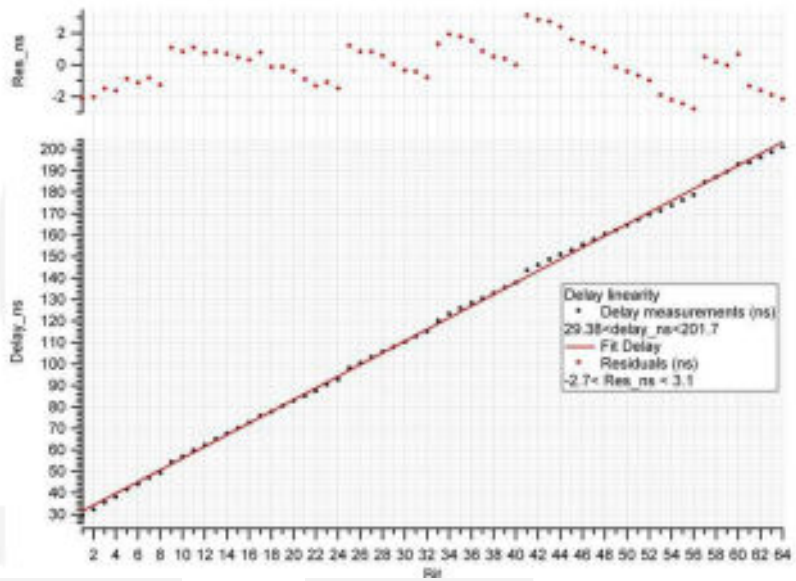


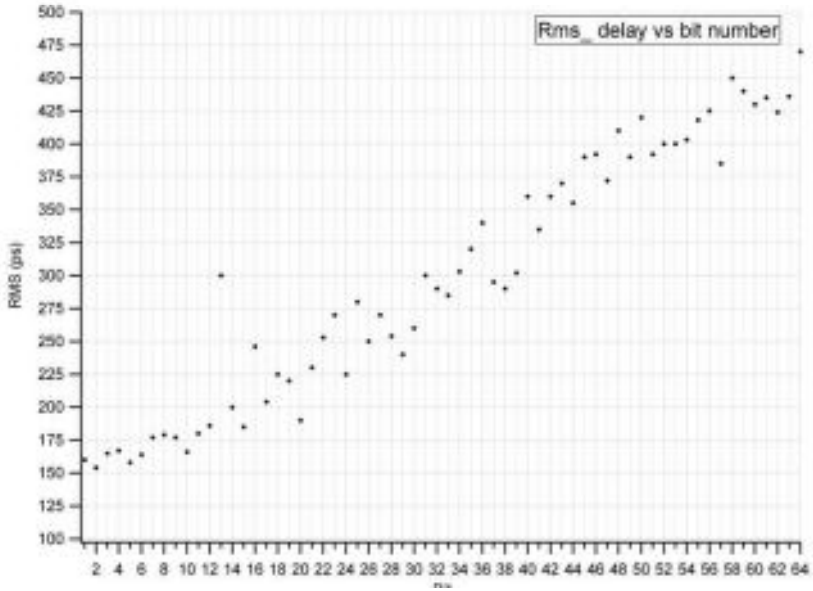




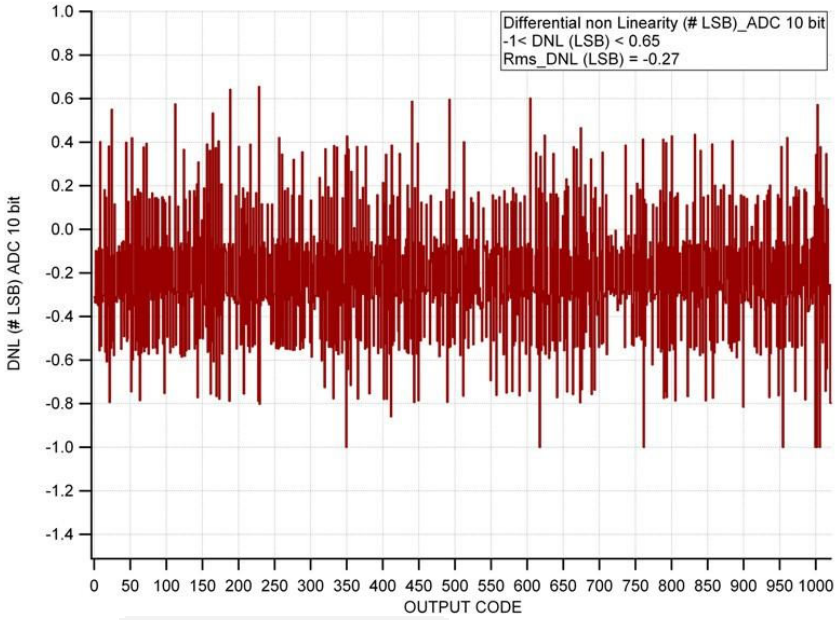
- Delay box to hold peak
  - 6 bits,
  - Span : 30-200 ns
  - step : 3 ns
  - Linearity : 1%
  - Jitter 150-450 ps

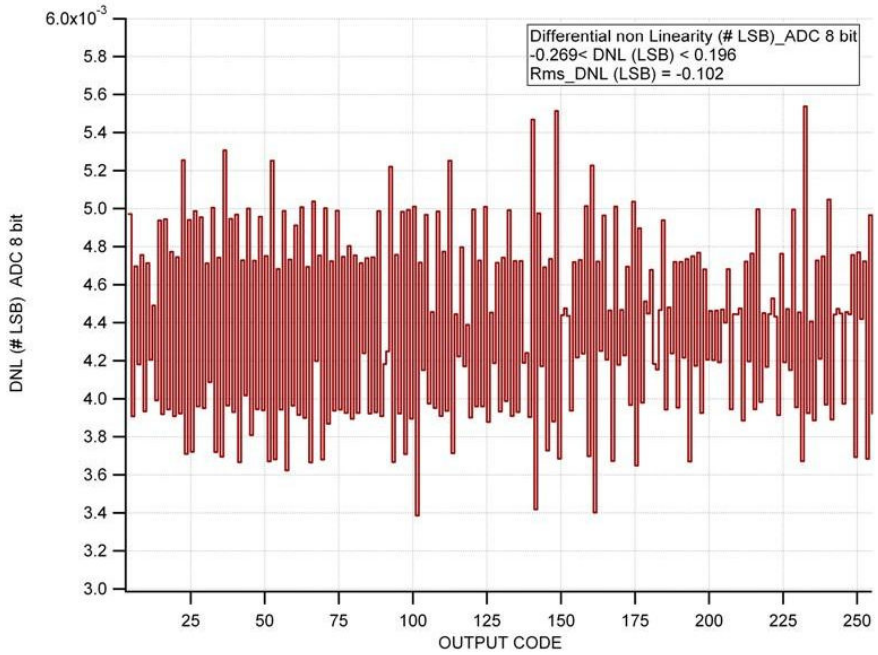






ADC DNL





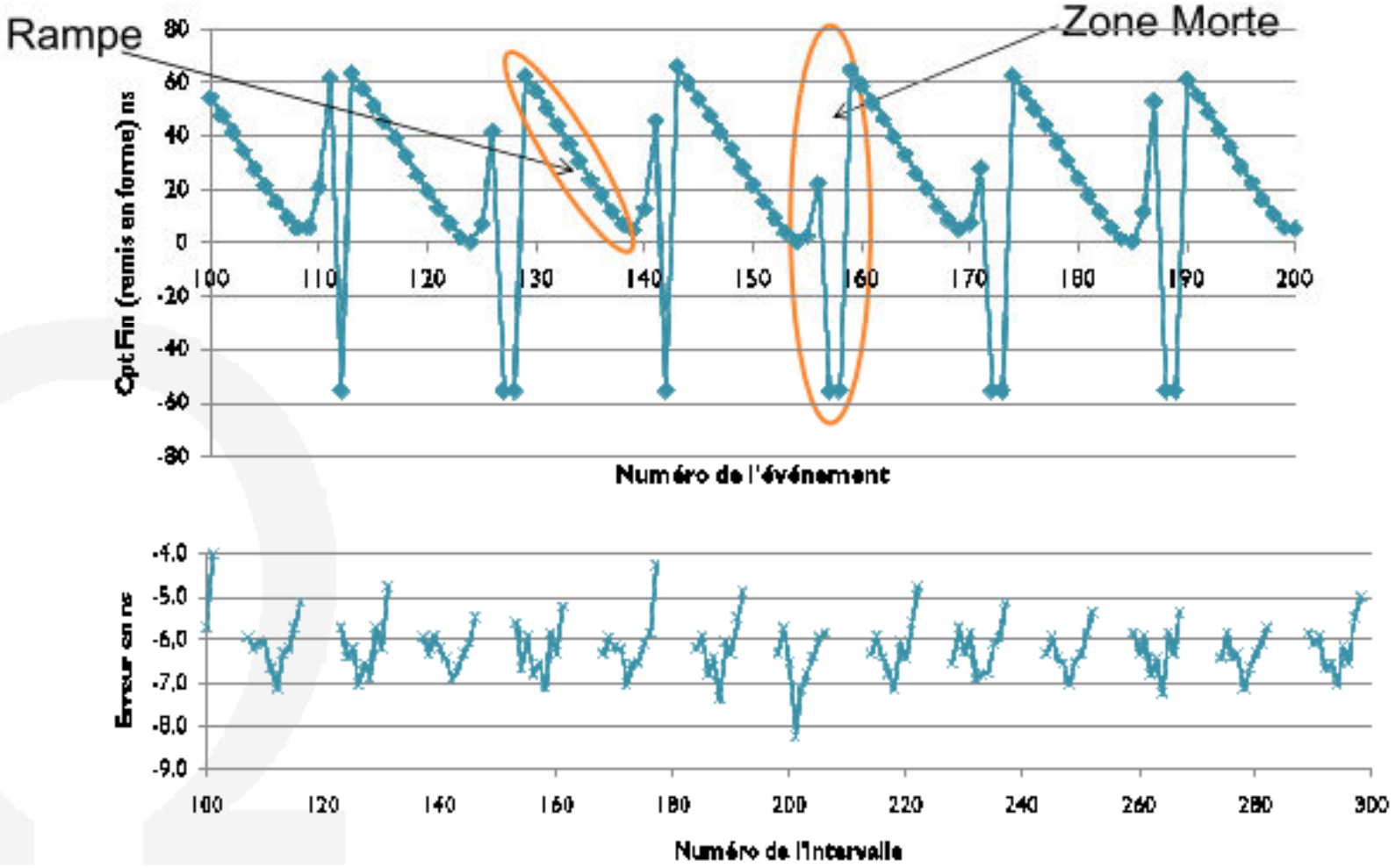
Preliminary results

Differential non linearity (DNL):
from -1 to 0.65 for the 10 bit ADC
from -0.3 to 0.2 for the 8 bit ADC

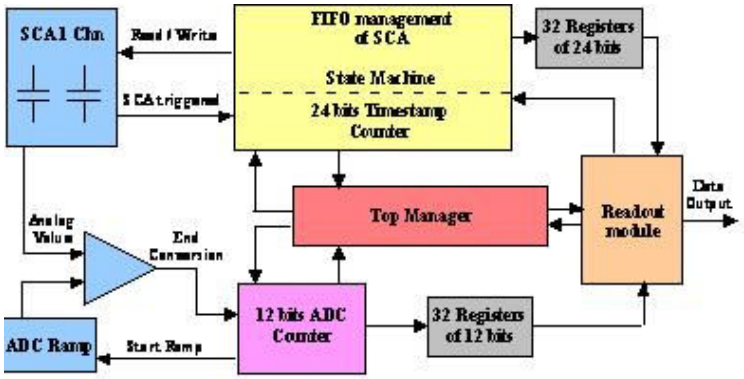
Fine TDC measurements

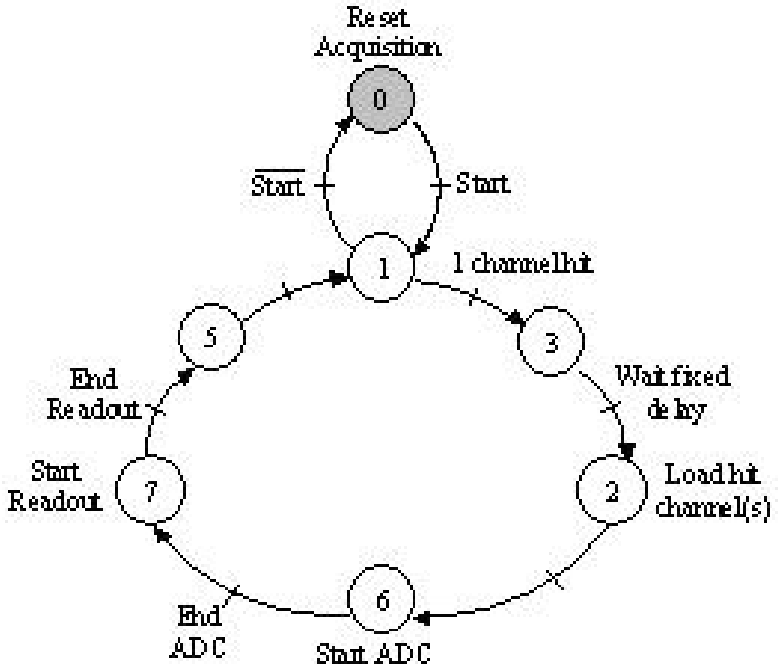
- Fine time digital data output
- Rms of clean part : rms = 0.62 ns

[S. Drouet IPNO]



Digital part





- Top manager module controls the 3 other ones: Acquisition, Conversion, Read out.
- When 1 or more channels are hit, it starts ADC conversion and then the readout of digitized data.
- The maximum cycle length is about 200 µs.
- During conversion and readout, acquisition is never stopped.