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PARISROC, a photomultiplier array integrated readout chip

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PARISROC is a complete read out chip, in AMS SiGe 0.35µm technology [1],for photomultipliers array. It allows triggerless acquisition for next generation neutrino experiments and it belongs to an R&D program funded by French national agency for research (ANR) and called PMm2:"Innovative electronics for photodetectors array used in High Energy Physics and Astroparticles"[2] (ref.ANR-06-BLAN-0186).
The ASIC integrates 16 independent channels with variable gain and provides charge and time measurement by a 12-bit ADC and a 24-bits Counter.

Summary

PARISROC is a front-end electronics ASIC designed for the next generation of neutrino experiments.
These detectors will take place in megaton size water tanks and will require very large surface of photodetection [3].
PMm2 project proposes to segment the very large surface of photo-detection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics. The ASIC must only send out the relevant data by network to the central data storage. This data management reduces considerably the cost of these detectors.
The PARISROC chip integrates 16 channels totally independents.
Each analogue channel is made of a low noise preamplifier with variable and adjustable gain. The variable gain is common for all channels. The gain is also tuneable channel by channel to adjust the input detector's gain (on 8 bit).
The preamplifier is followed by a slow channel for the charge measurement in parallel with a fast channel for the trigger output.
The slow channel is made by a variable (50-200ns) slow shaper followed by an analogue memory with depth of 2 to provide a linear charge measurement up to 50pC; this charge is converted by a 12 bit Wilkinson ADC.
The fast channel is composed of a fast shaper (15ns) followed by 2 low offset discriminators to auto-trig down to 10fC. The thresholds are loaded by 2 internal 10-bit DACs common for the 16 channels. The 2 discriminator outputs are multiplexed to provide only 16 trigger outputs. Each output trigger is latched to hold the state of the response until the end of clock cycle. It is also delayed to open the hold switch on the maximum of the slow shaper.
On each channel, a fine time measurement is made by an analogue memory with depth of 2 which sample a 12 bit ramp, common for all channels, as the same time of the charge. This time is then converted by a 12 bit Wilkinson ADC.
The two ADCs discriminators have a common ramp, of 8, 10 or 12 bits, as threshold to convert the charge and the fine time.
A bandgap bloc provides all voltage references.
A digital part [4] manages all the acquisition, the conversion and the readout and provides by a 24-bit counter the coarse time measurement or timestamp.
Design, simulation results and measurements of the first prototype will be presented.

References:
[1] http://asic.austriamicrosystems.com/
[2] http://pmm2.in2p3.fr/
[3] B. Genolini et Al., PMm2: large photomultipliers and innovative electronics for next generation neutrino experiments, NDIP'08 conference.
[4] F. Dulucq et Al., Digital part of PARISROC: a photomultiplier array readout chip, TWEPP08 conference.

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