Contribution ID: **67** Type: **Oral**

The GBT project

Thursday, 24 September 2009 11:00 (25 minutes)

The GigaBit Transceiver (GBT) architecture and transmission protocol has been proposed for data transmission in the physics experiments of the future upgrade of the LHC accelerator, the SLHC. Due to the high beam luminosity planed for the SLHC the experiments will require high data rate links and electronic components capable of sustaining high radiation doses. The GBT ASICs addresses this issue implementing a radiation-hard bi-directional 4.8 Gb/s optical fibre link between the counting room and the experiments. The paper describes in detail the GBT architecture and will present an overview of the various components that constitute the GBT chipset.

Summary

The GBT collaboration is working on the development of a full-custom radiation-hard chipset (the GBT chipset) to implement high-speed (4.8 Gb/s) optical links between the counting room and the experiments' sub-detectors. The GBT will implement point-to-point duplex links allowing bidirectional data transmission between the counting room and the detectors. It is designed so that the large bandwidth of a single optical fibre link can be shared among several frontend devices by providing up to 40 electrical links (E-Links) between the GBT chipset and the frontend ASICs. These E-Links are bit rate programmable and will thus accommodate different requirements in terms of bandwidth and number of interconnects between the frontend ASICs and the GBT chipset. The flexibility provided by the possible E-Link configurations will easily allow the GBT chipset to serve a variety of detector topologies and bandwidth requirements.

The GBT architecture is tailored to support simultaneous transmission of physics, trigger and experiment control data over the same link. The GBT will act thus simultaneously as a data-link and as a TTC transceiver incorporating many of the functions that traditionally have been separated physically and functionally in data-acquisition, timing, trigger and experiment control links.

Due to the high beam luminosity of the SLHC the radiation doses are expected to reach the 100 Mrad level for some of the inner detectors. These high levels of radiation will pose long term reliability problems to the electronics due to total dose effects which can be minimized by using advanced CMOS commercial technologies and by following special layout techniques previously developed for the LHC ASICs. The GBT ASICs will be thus fabricated in a commercial 130 nm technology which will ensure the required radiation tolerance.

The high luminosity will also be linked to a high rate of the Single Event Upsets (SEU). These are a major impairment to error free data transmission at high data rates. To deal with this situation the GBT adopts a robust error correction scheme that will allow the correction of bursts of errors caused by SEUs on photodiodes and on the electronic circuits. The data communications protocol was chosen so that it is possible to develop compatible firmware in most standard FPGAs existing today in the market thus enabling the implementation of GBT compatible transceivers within FPGAs mounted in the counting rooms where radiation tolerance is not required.

The development of this architecture has gained acceptance among the High Energy Physics (HEP) community working for SLHC and the project has been approved as DG white paper project in 2008. During 2008 to date several ASIC and FPGA developments have taken place that will be introduced in the paper. The proposed architecture, the communications protocol will be described in detail and the project organization and schedule will be presented.

Primary author: Mr MOREIRA, Paulo (CERN)

Presenter: Mr MOREIRA, Paulo (CERN)

Session Classification: Parallel Session B5 - Optoelectronics and Links

Track Classification: Optoelectronics and Links