Presentation of the "ROC" chips readout

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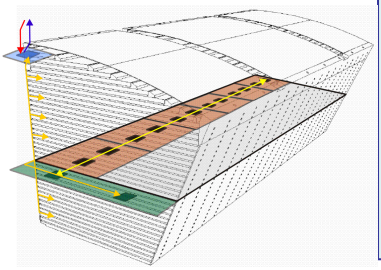
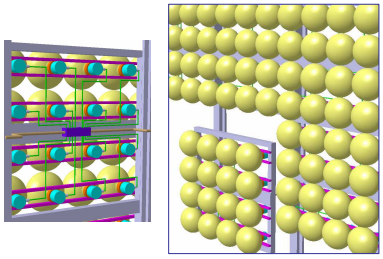
SPIROC: ILC AHCAL calorimeter



Abstract:

The OMEGA group at LAL has designed 3 chips for ILC calorimeters: one analog (SPIROC) and one digital (HARDROC) for the hadronic one and also one for the electromagnetic one (SKIROC). The readout and the management of these different chips will be explained.
To minimize the lines between the ASICs and the DAQ, the readout is made thanks to 2 lines which are common for all the chips: Data and TransmitOn. As the chips are daisy chained, each chip is talking to the DAQ one after the other. When one chip has finished its readout, it starts the readout of the chip just after. Moreover, during this readout, only the chip which is talking to the DAQ is powered: this is made thanks to the POD (Power On Digital) module in the ASIC. In the ILC mode, readout sequence is active during inter bunch crossing (like ADC conversion).
Another chip designed for PMM2 R&D program (PARISROC) integrates a new selective readout: that's mean only hit channels are sent to the DAQ in a complete autonomous mode.

PARISROC: Module of 16 PMTs



Overview of ROC chips

MAROC

MAROC (Multi-Anode ReadOut Chip) is designed to read multi-anode photomultipliers of the ATLAS luminometer made of Roman pots.

SKIROC

SKIROC (Silikon Kalorimeter ReadOut Chip) has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements.

HARDROC

HARDROC (HAdronic Rpc Detector ReadOut Chip) is the front end chip designed for the readout of the RPC or GEM foreseen for the Digital HAdronic CALorimeter of the future ILC.

SPIROC

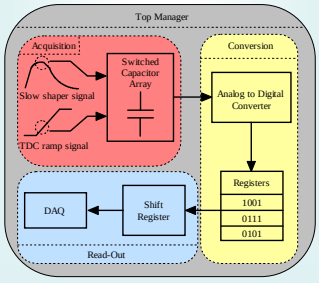
SPIROC (SiPM Integrated ReadOut Chip) is a dedicated front-end electronics for an ILC prototype of hadronic calorimeter with Silicon photomultiplier readout.

PARISROC

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments.

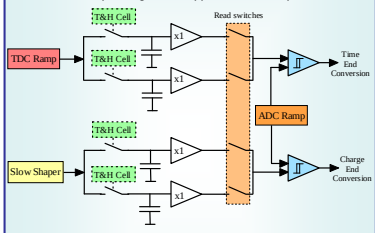
High level working of ROC chips

The ROC chips can be divided in 2 groups: analog and digital ones. It depends if the signal from the detector is first stored into a analog way or directly in a digital way.
For analog chips, discriminated analog signals are first stored into an analog memory (the SCA: switched capacitor array) and then converted into digital word thanks to an ADC. These digital values are stored in a RAM to be readout at the end of the acquisition cycle.
For digital chips, the ADC is not needed as data are directly saved into the RAM.

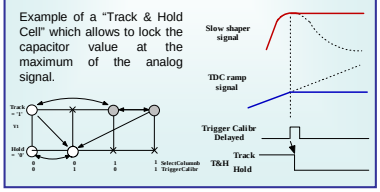


Main block of analog ROC chips: SCA

These analog chips are based on SCA. The number of channels managed can be up to 64. Fine time measurement is available depending on the application and experiment.

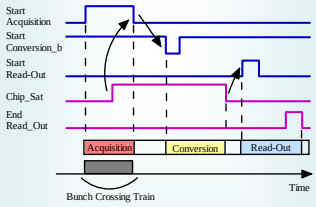


Example of a "Track & Hold Cell" which allows to lock the capacitor value at the maximum of the analog signal.



Global timing considerations

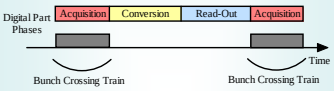
Depending on the application, acquisition module is not active all the time. For example, in bunch crossing train sequence like in the future ILC, acquisition is stopped after each train. This is the case for SKIROC, SPIROC and HARDROC chips for ILC calorimeters.



In neutrino experiment, acquisition is never stopped. This is the case for PARISROC chip which can handle an acquisition active all the time. During its conversion and readout phases, discriminated analog signals can be stored in the SCA if it is not full.

Future ILC timing considerations

Future ILC is based on a 200ms bunch crossing train period. For the font end electronics, the digital part of acquisition is active only during the bunch crossing and the conversion and the readout are active during inter bunch crossing.



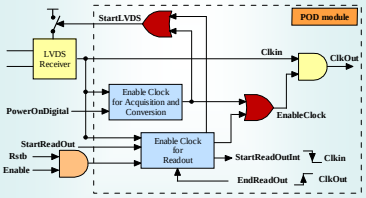
Acquisition and conversion module are active at the same time for all the ASICs. That's why the power on can be managed by the DAQ. But, as the readout is daisy chained, the power on should also be managed by the daisy chain. On the table below are represented the maximum duration of each phases.

Module / Phase	Duration	Comments
Acquisition	1ms	Bunch crossing train duration
Conversion	3ms	Worst case (32 conversions)
Readout	4ms	5 MHz readout clock

For each cycle of 200ms, one ASIC should be powered only 8 ms (4% of cycle). This will allow to meet power budget. POD module was designed to fulfil this requirement for the digital part.

POD Module Block Diagram

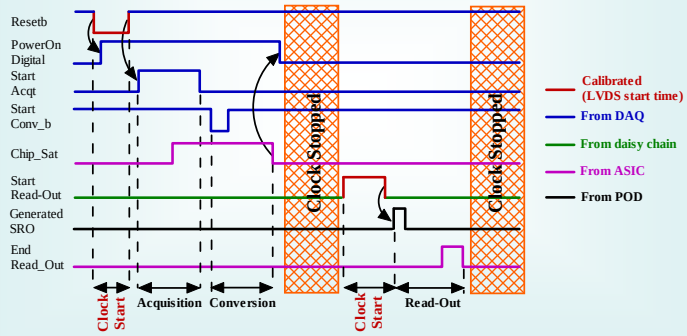
Power On Digital (POD) module has been design to meet ILC power budget for front end electronics. Il allows to start and stop clocks depending on the 3 phases (acquisition, conversion and readout).
Additionally with start/stop of the clock, it manages the LVDS receiver bias current: its power supply. The combination of clock gating and LVDS management allows to meet the power budget of the ILC.



The POD module is divided in 3 parts. One is activated and managed by the DAQ during common phases: acquisition and conversion. The second one is set during the readout by the daisy chained token. The last one manages the LVDS receiver.

POD module detailed diagram

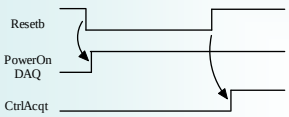
The timing diagram given below represents the complete sequence driven by the DAQ. It shows the 3 sequences and how they are managed. The "clock stopped" zones corresponds when POD is off (not scaled). As mentioned above, it represents 96% of time and allows to meet power budget requirement (25 uW per channel). For each phases, clock is started asynchronously, enabled and stopped synchronously (idle state at logic '0').



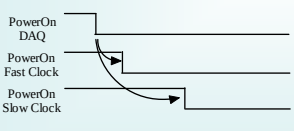
POD internal management

Acquisition and Conversion phases:

PowerON is set during the reset phase before each acquisition. It allows to start the LVDS receiver and consequently the clocks. When clock are established, reset can be released, this is done after reset startup time which is about 200 ns. That's why reset duration must be longer than LVDS wakeup time.



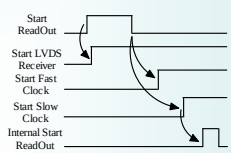
PowerON is released at the end of the conversion. It is synchronized internally to properly stop the clocks. Effective PowerOn release is done after few clock ticks (2-3).



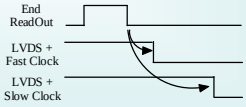
PowerON is asynchronously set by the DAQ during the reset state and it is synchrnously released by the POD in each chips.

Readout phase:

PowerON during daisy chained readout is done by the previous chip thanks to its calibrated EndReadout which is the StartReadout of the chip just after it. This signal allows to start LVDS receiver and then synchronously the clocks. Finally, it generates an internal StartReadout for state machines.



At the end of the readout, clocks and LVDS receivers are stopped synchronously. Effective PowerOn release is done after few clock ticks (2-3).



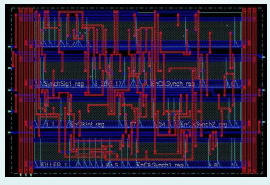
POD Layout

POD has been layouted with standard 3-b cells from AMS (Austria Micro System). The main layout features are given after:

- Area : 120 um x 80 um
- 8 Flips Flops
- 2 metals (M1and M2)
- Compliant with a clock up to 40 MHz

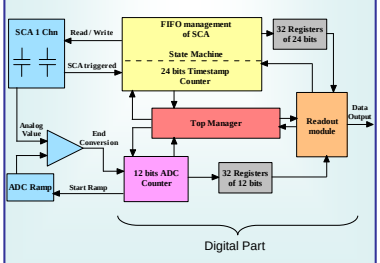
Besides, power supply pins are accessible at each corner of the module (Vdd, Gnd and Vss).

This module has been integrated in HARDROC chips at revision 2 and higher.



Parisroc new readout

Parisroc integrates a state machine to control the 3 phases: it allows to have a complete autonomous working. Moreover, compare to other ROC chips, it integrates a new channel management: they are completely independent. That's mean, when 1 channel is hit, ADC conversion is started and then the readout of this channel. The readout will only treat hit channels, that's why this module tags each frame with its channel number.
During conversion and readout, acquisition is never stopped: triggers are stacked into SCA and treated as soon as possible.



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