FPGA-based Bit-Error-Ratio Tester for SEU-hardened Optical Links

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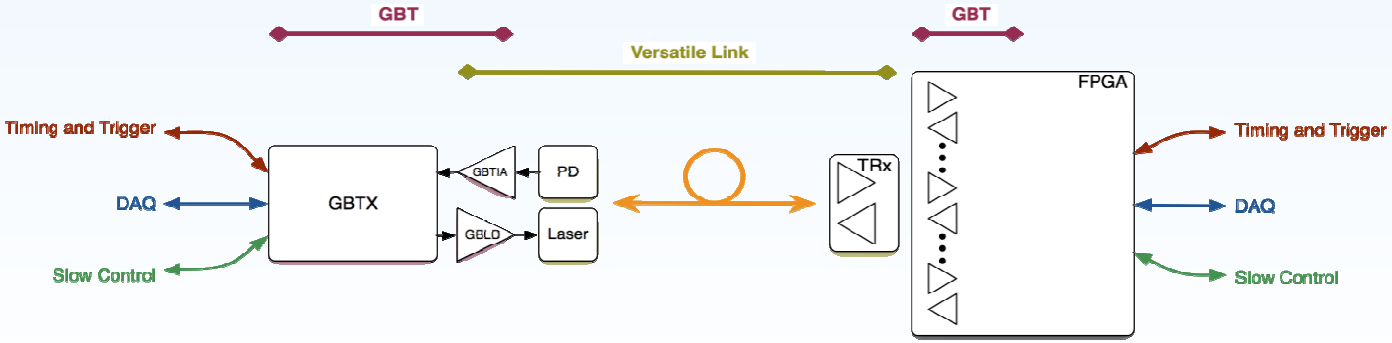
CERN, PH-ESE

Introduction

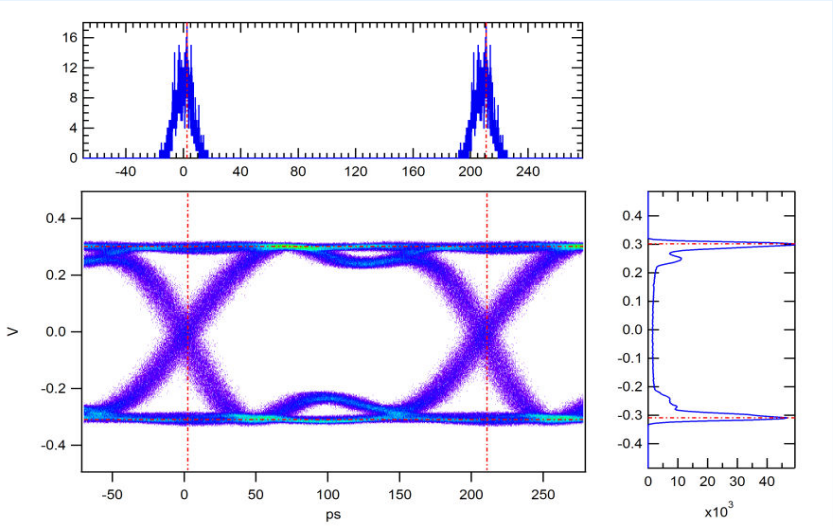
- Stringent requirements
  - High speed, low power, high reliability, long lifetime etc.
- Harsh environment
  - Noise, radiation etc.

- The answer: Versatile Link and GBT projects

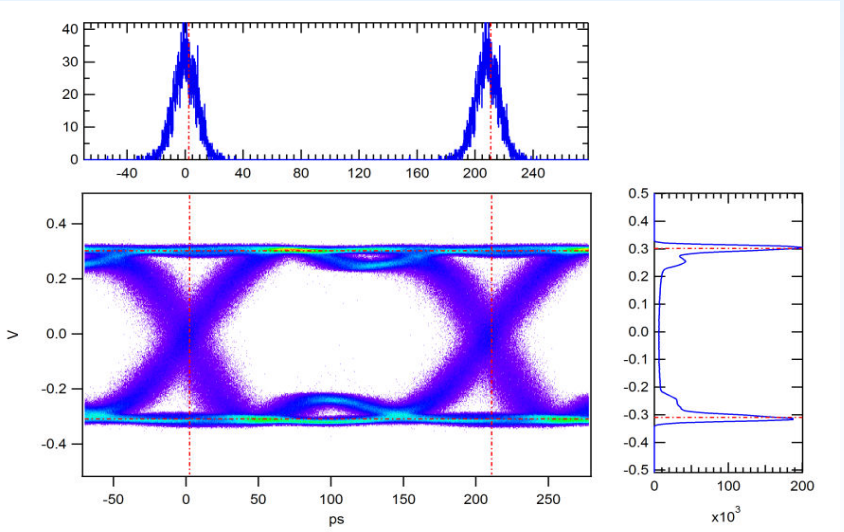


Challenges (1/2)

- Amplitude noise
  - Low-swing signals => reduced SNR
- Phase noise, i.e. Jitter
  - Reduced bit period => less tolerance



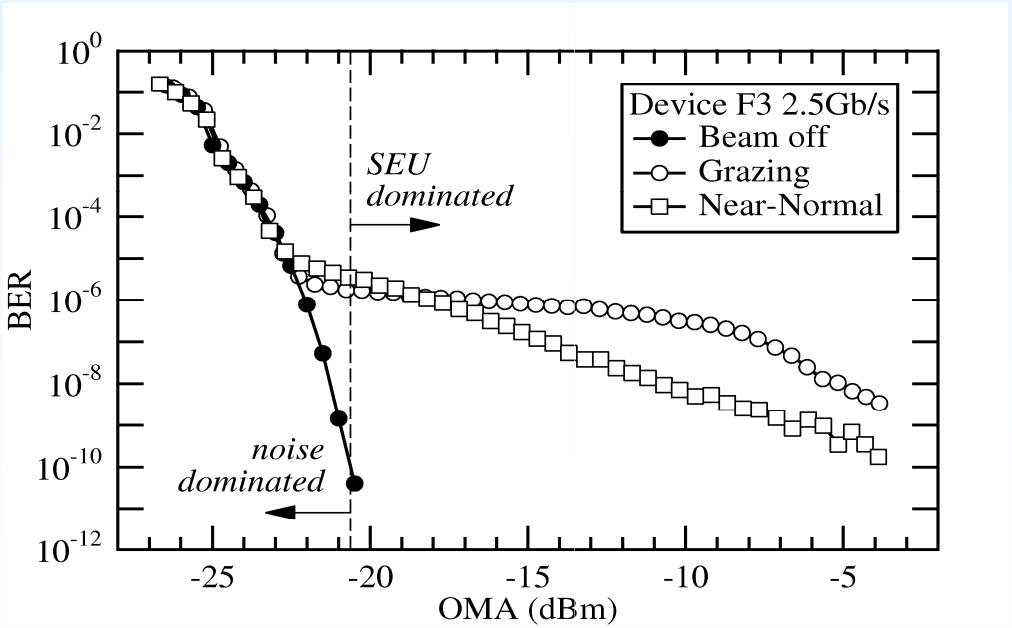
Receiver electrical signal



Receiver electrical signal, when the optical signal is attenuated

Challenges (2/2)

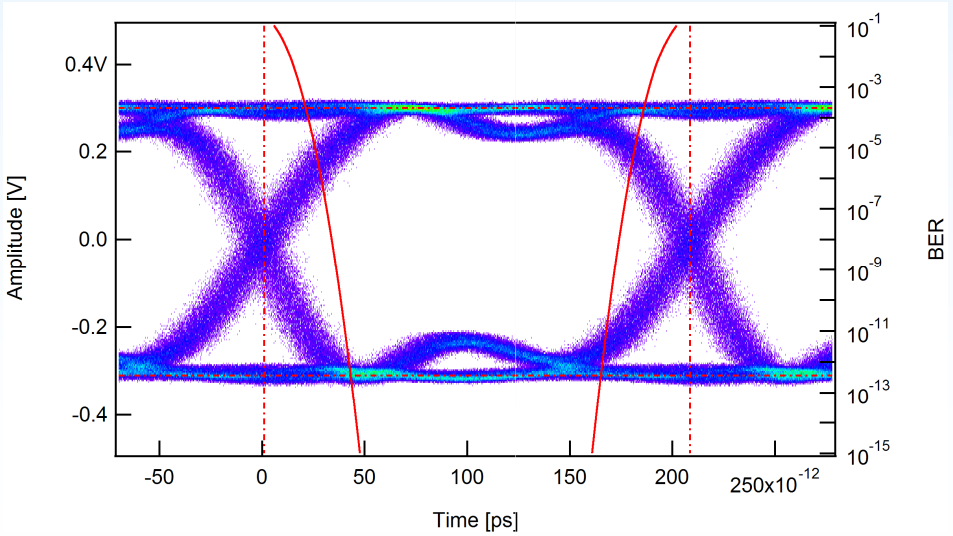
- Radiation effects
  - Single-Event Upsets in the photodiode and in the receiver subassembly
  - In the SEU dominated region, the BER is almost independent from the SNR



Jan Troska et al., "Single-Event Upsets in Photodiodes for Multi-Gb/s Data Transmission", TWEPP 2008, Naxos, Greece

Test methods

- Eye diagram
  - Good qualitative measurement
  - Difficult to predict the bit error rate
  - Used for mask tests (standards)
- Bathtub curve
  - Links the jitter performance to the bit error rate
  - Ignores the amplitude noise
  - Not precise at low bit error rate (extrapolation)



Bit Error Rate testing

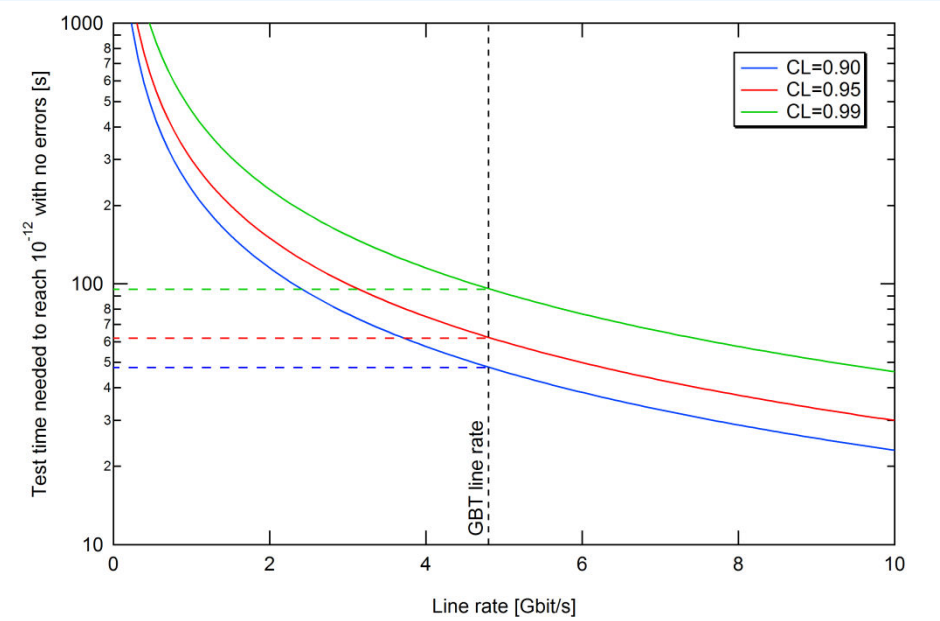
- Simple method for evaluating the performance of the entire transmission channel

$$BER = \frac{N_{err}}{N_{bits}}, \text{when } T \to \infty$$

- The measurement time depends on the required confidence level and the number of errors observed

$$T = -\frac{\ln(1-CL)}{BER * R} + \frac{\ln(\sum_{k=0}^{N} \frac{(n * BER)^k}{k!})}{BER * R}$$

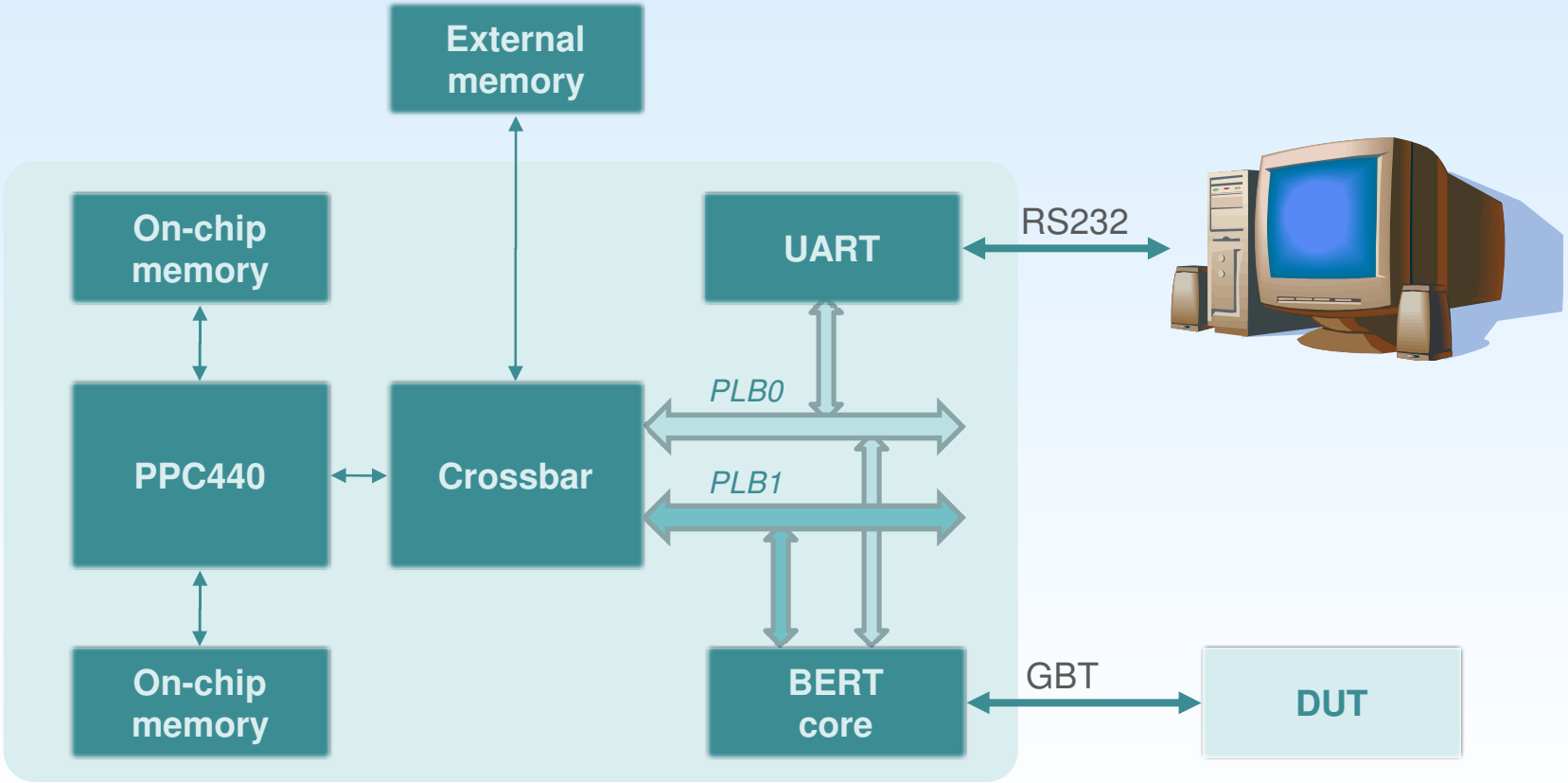
T	*– measurement time*
BER	*– target bit error rate*
R	*– data rate*
CL	*– confidence level*
n	*– number of transmitted bits*
N	*– number of error bits*



Motivations to build a custom BERT

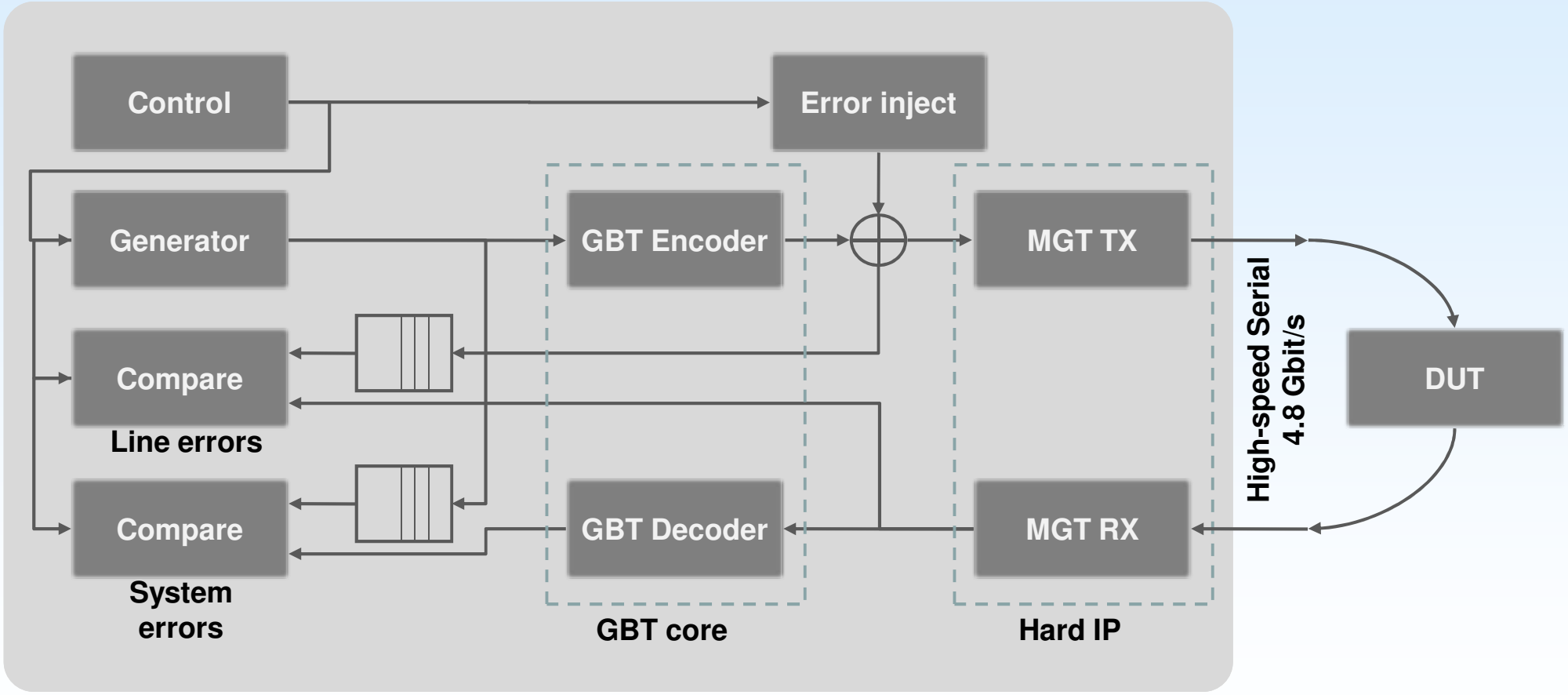
- Limitations of the oscilloscope
  - Sampling rate, memory, extrapolation, long measurement time
- We would like to use custom physical layer protocol (GBT)
  - It will allow us to study the performance of the protocol
  - Standard BERT uses pseudo-random bit pattern
- We would like to carry out tests on multiple channels
  - It will reduce the overall test time
  - Standard BERT can typically handle one channel at a time
- Error logging
  - Required for off-line analysis
  - Limited in standard BERT equipments

BERT system architecture



SoC implemented on the ML523 Virtex 5 transceiver evaluation platform

Bit Error Tester – Single Channel



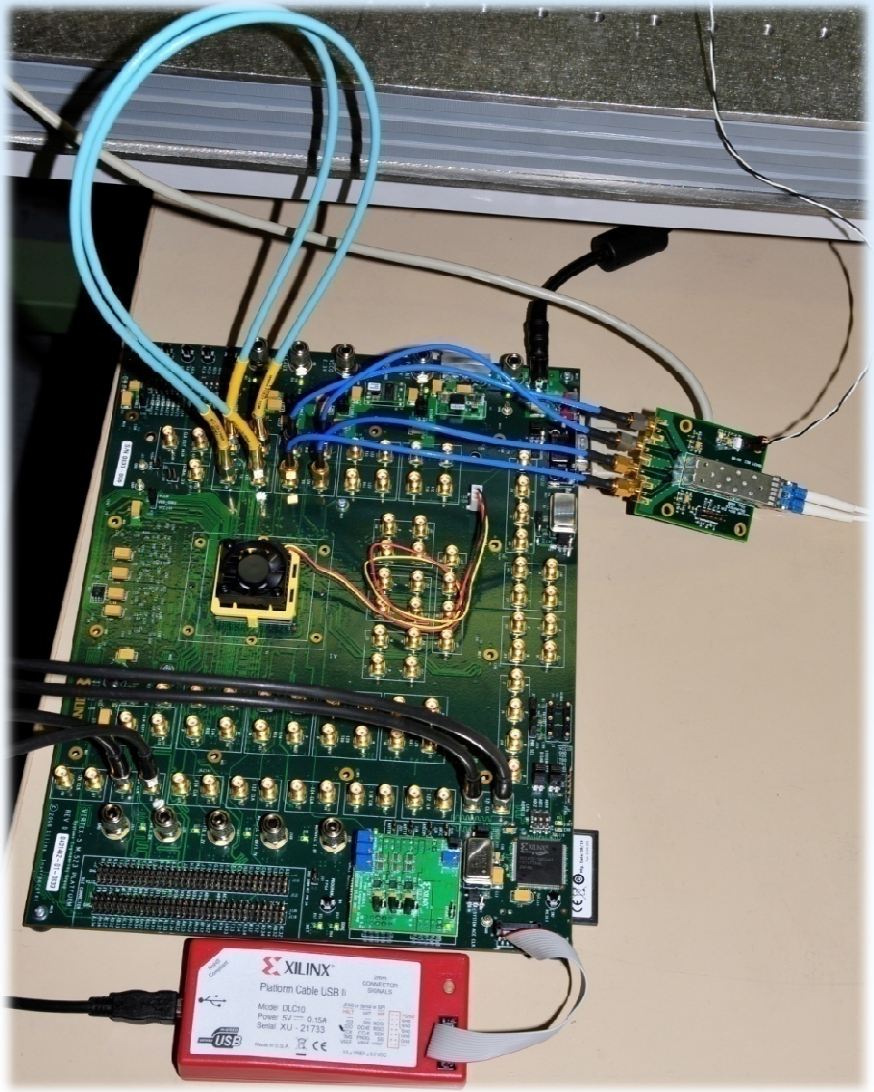
Development platform

ML523 Virtex 5 transceiver evaluation platform featuring:

XC5VFX100T device
- 8 GTX dual tiles
- 16,000 slices
- 256 DSP48E blocks
- 8,208,000 bits internal memory

+

128 MB DDR2 external memory



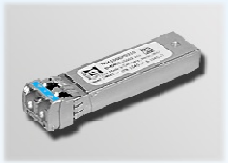
Test system

J-BERT
N4903A

Clock source

BERT

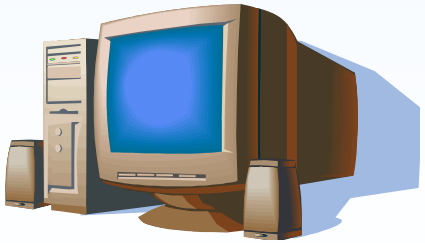
electrical



optical

Attenuator

Agilent
8156A



Labview

Power meter

Agilent
8163B + 81635A

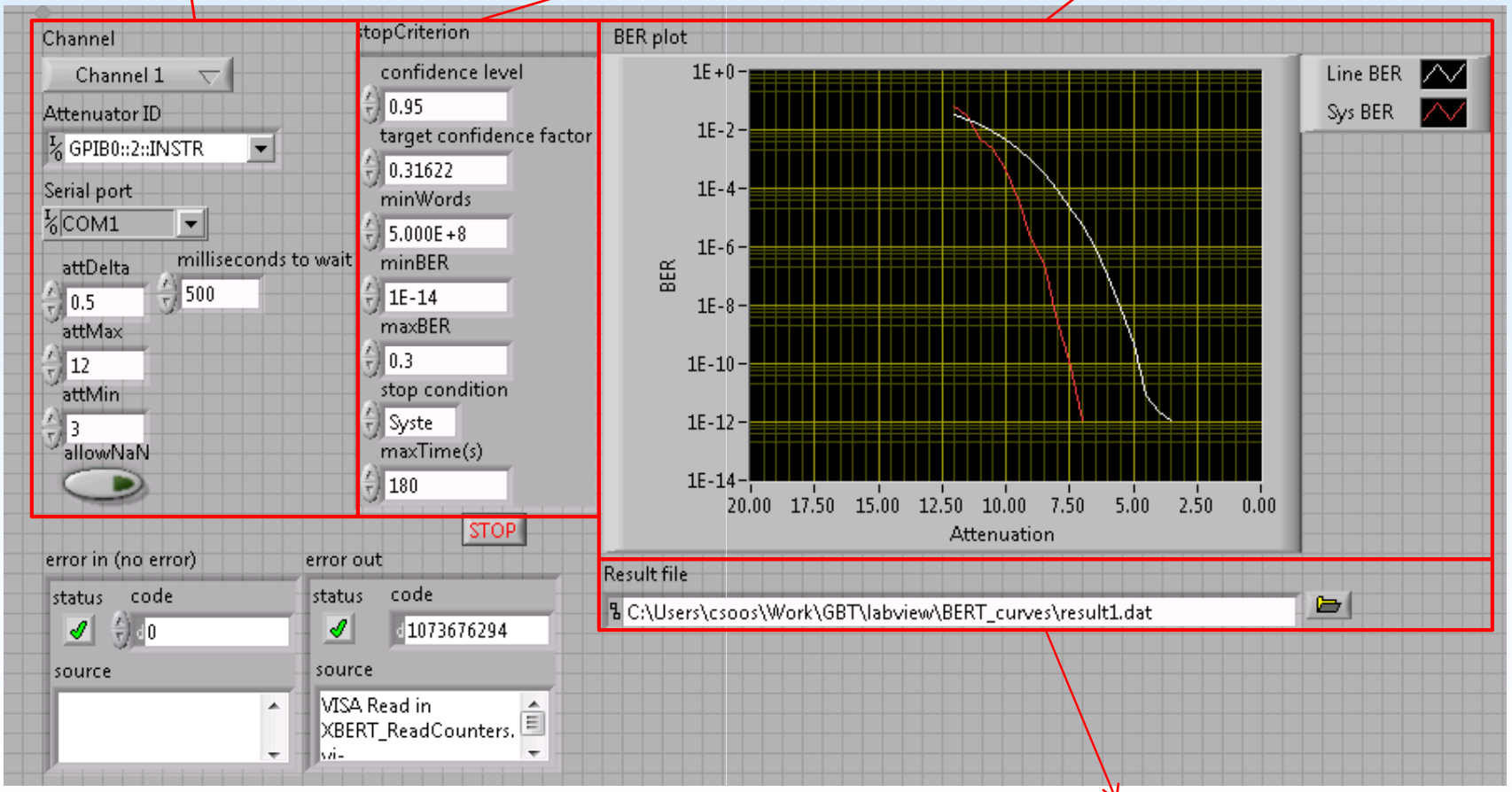
Graphical user interface - Labview

Versatile Link

Measurement settings

Stop criteria

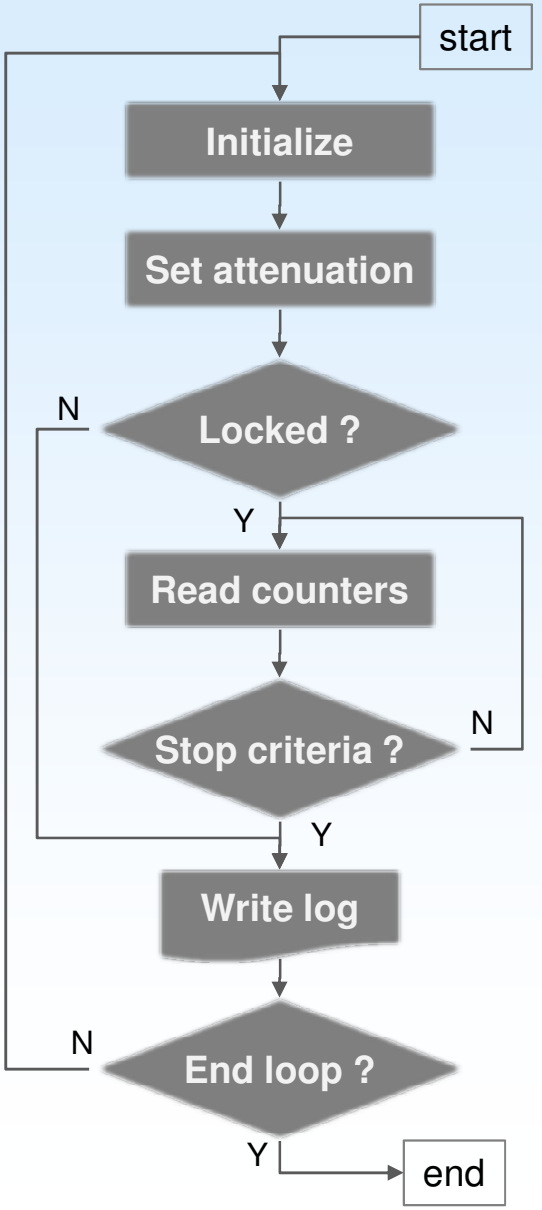
Result plots



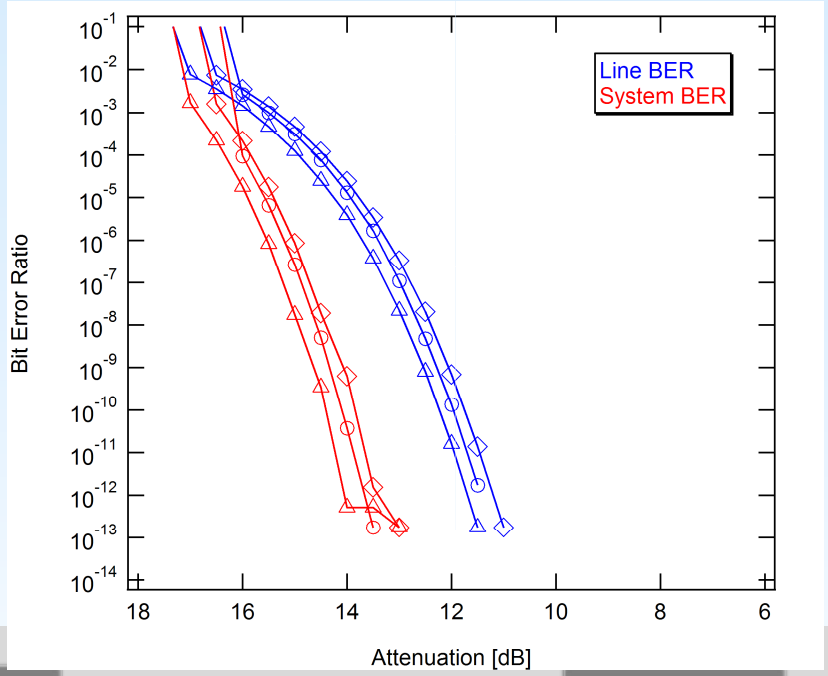
Log file path

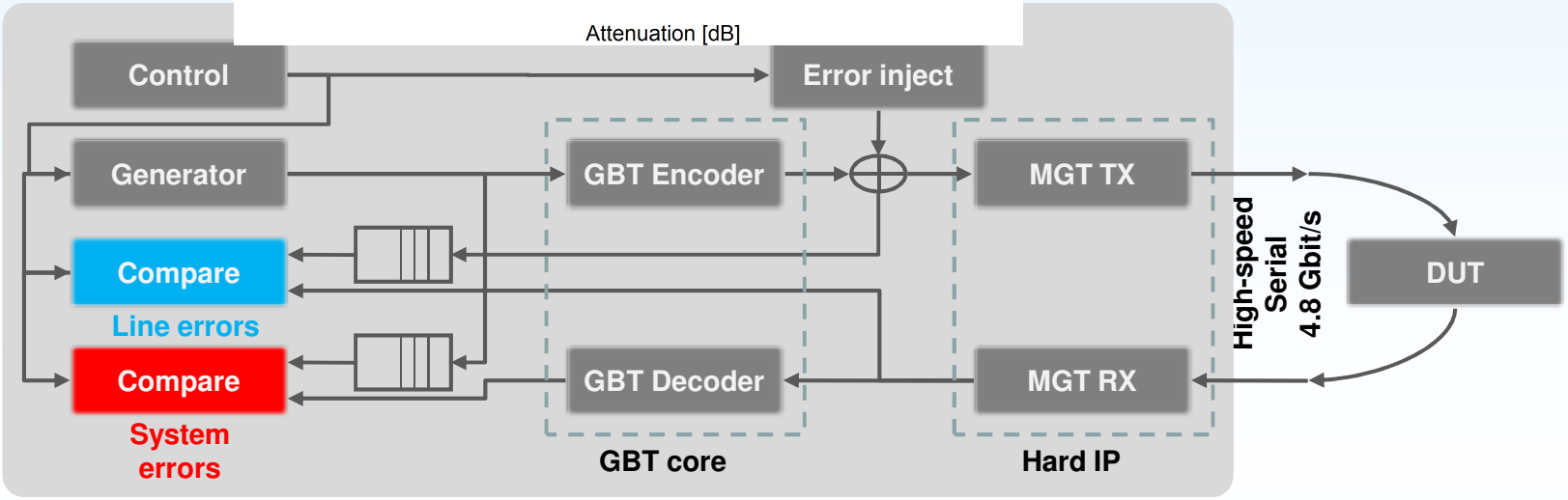
Measurement flowchart

- To improve speed, measurements are started from the highest attenuation value
- If a channel cannot acquire lock, it will be masked
- Stop criteria: target BER, confidence factor, time
- Record values: BER bounds, confidence factor, time, average optical power
- The loop is finished, when we reach the target BER on all channels

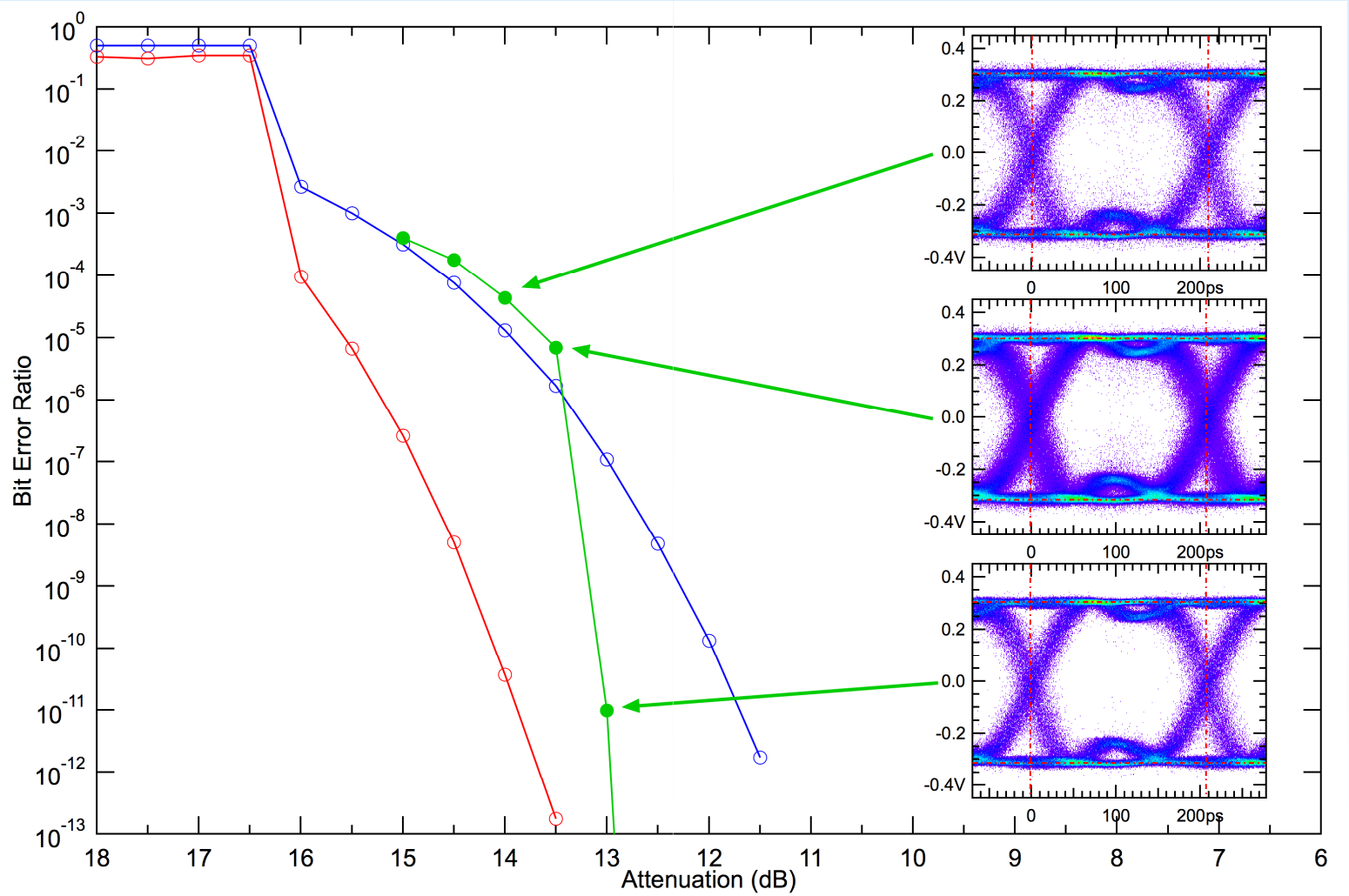


Results – System and Line BER





Results – Scope vs. BERT



Future work

- Optimize the system for multi-channel readout
  - FPGA resource usage (clock network and PLLs)
  - Labview script
- Implement advanced logging
  - Record erroneous words with timestamp
- Add support for multiple line rates
  - Dynamic reconfiguration of the multi-gigabit transceivers
- Prepare the system for the SEU tests
- Test components in radiation

Conclusion

- Future, radiation-hard optical links will have to meet strict requirements
- The physical layer protocol will have to deal with the radiation induced errors (GBT)
- Bit-Error-Rate testing can be used to characterize the link components quantitatively
- Advanced testing (error logging) can provide insights into how error propagates in the system
- FPGA-based BERT system supporting the above mentioned features has been developed
- Link components are being tested in the lab, and will be tested soon (November 2009) in radiation

Thank You !

System architecture – Virtex 4