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FPGA-based Bit-Error-Ratio Tester for SEU-hardened Optical Links

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Reliable optical links for future High-Energy Physics experiments will require components qualified for use in radiation-hard environments. To cope with radiation induced single-event upsets, the physical layer protocol will include Forward Error Correction (FEC). Bit-Error-Ratio (BER) testing is a widely used method to characterize digital transmission systems. In order to measure the BER with and without the proposed FEC, simultaneously on several devices, a multi-channel BER tester has been developed. This paper describes the architecture of the tester, its implementation in Xilinx FPGA devices and discusses the experimental results.

Summary

In the framework of the Versatile link project [1], optical transceiver components will be tested to verify their compliance with the requirements of future radiation hard optical links in High-Energy Physics experiments. A widely accepted method to test digital transmission systems and their components is the Bit-Error-Ratio (BER) test. In order to quantify the effects of radiation the components will be irradiated and the impact of the Single-Event Upsets (SEU) on the BER will be investigated.

Measuring the BER with high confidence level (> 0.95) is usually a lengthy process, thus testing components sequentially takes too much time. Therefore, a multi-channel BER Tester (BERT) supporting the measurement of several components simultaneously has been developed. The BERT operates at multiple data rates up to a maximum of 6.5 Gbit/s. Unlike standard equipment that uses pseudo-random bit patterns, the BERT described uses the custom physical layer protocol, which is proposed by the GigaBit Transceiver (GBT) project [2]. In order to cope with the radiation induced SEUs, the protocol will include Forward Error Correction (FEC). By measuring the BER both before and after the error correction, the tool can be used to evaluate the performance of the FEC in the radiation environment.

Detailed information about the architecture, the implementation in Xilinx Virtex-4 and Virtex-5 FPGA devices, as well as a procedure to improve the measurement time will be discussed in the paper. Results of laboratory BER tests of standard components will be shown for reference and finally results from the SEU tests will be presented.

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