Hardware studies for the upgrade of the ATLAS Central Trigger Processor

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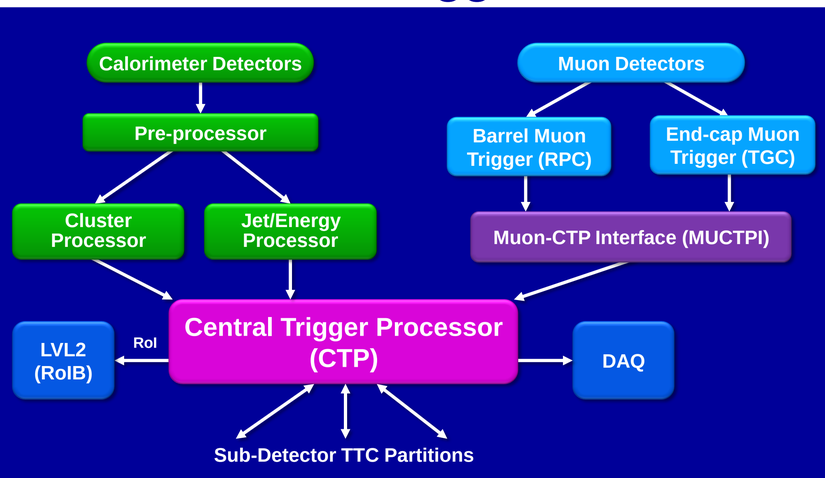
ATLAS Level-1 Trigger Overview



The ATLAS Central Trigger Processor (CTP) is the final stage of the first level trigger system which reduces the collision rate of 40 MHz to a Level-1 event rate of 75 kHz. The CTP makes the Level-1 trigger decision based on multiplicity values received from the calorimeter and muon trigger systems using programmable selection criteria. It also receives trigger inputs from various other sources, including luminosity detectors, minimum-bias trigger scintillators and beam pick-ups. In addition the CTP sends trigger summary information to the Level-2 trigger and the data-acquisition systems and provides accumulated and bunch-by-bunch scaler data for monitoring of the trigger, detector and beam conditions.

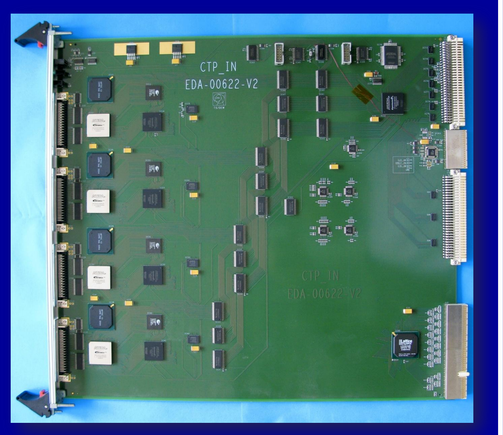
In order to improve the rejection rate for the first phase of the planned luminosity upgrade of the LHC to $3 \cdot 10^{34}$ cm^{-2} s^{-1}, one of the options being studied consists of adding a topological trigger processor, using Region-Of-Interest (RoI) information from the calorimeter and potentially also the muon trigger. This will require an upgrade of the CTP in order to accommodate the additional trigger inputs. The constraint for the upgrade study presented here was to reuse the existing hardware as much as possible. This is achieved by operating the backplane at twice the design frequency and required developing new FPGA firmware for several of the CTP modules.

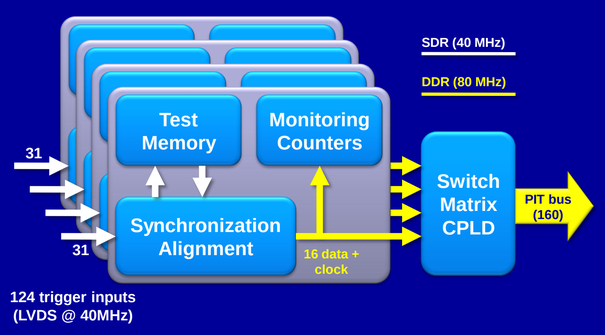
CTP Input Module (CTPIN)

The CTPIN has four identical channels, which receive 31 LVDS trigger input signals at 40 MHz each. After level conversion, an FPGA synchronizes the trigger inputs with respect to the internal clock, aligns them with respect to each other using programmable length pipelines and optionally checks their parity. The synchronized trigger inputs can be stored in a diagnostic memory for debugging and monitoring purposes. This functionality is implemented in an Altera Stratix FPGA (EP1S20).

An Altera Cyclone FPGA (EP1C20) is used to monitor the trigger inputs with counters that integrate over all bunches. Each channel also features a TDC (CERN HPTDC ASIC) to measure the phase of each trigger input signals.

Finally a configurable switching matrix implemented in a Lattice CPLD (ispXPLD) is used to select and route the aligned trigger inputs to be sent to the PIT bus. The internal clock of the CTPIN module can be adjusted using a programmable delay line (CERN DELAY25 ASIC).

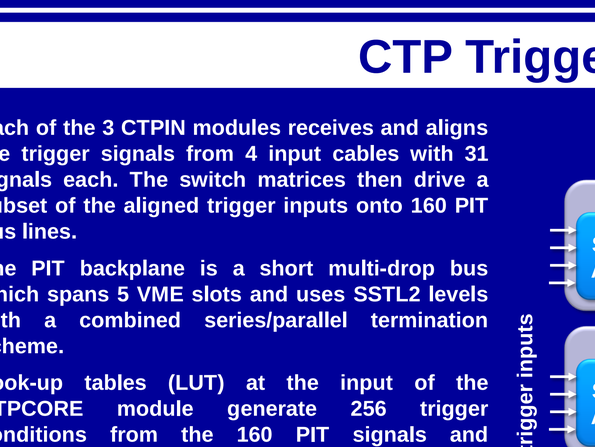


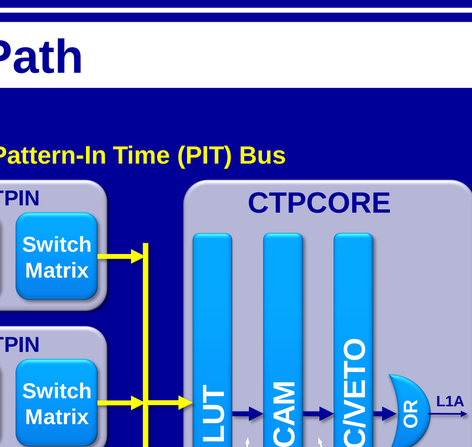


The modified firmware of the synchronization and alignment FPGA features DDR output registers which drive the 31 trigger signals onto 16 DDR lines. Since the monitoring FPGA connects to the same lines, DDR input registers were added there. In addition a 90° phase shifted clock is sent to the monitoring FPGA in order to correctly latch the DDR signals.

The 16 DDR output signals of each channel are sent to the switch matrix CPLD which selects and routed the 64 lines from the CTPIN onto the 160 PIT bus lines.

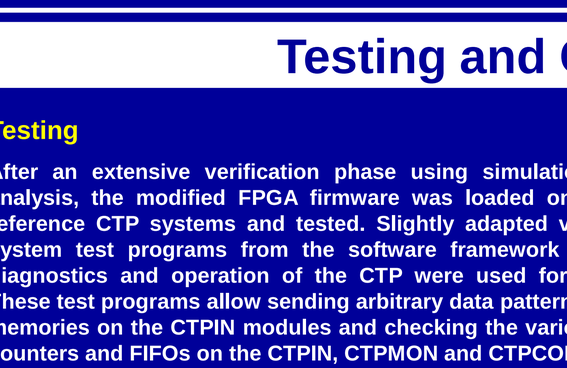
CTP Architecture & Implementation

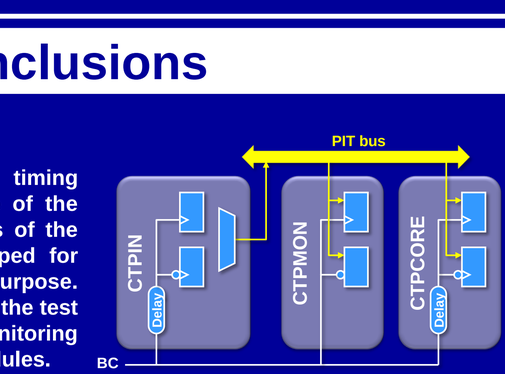




The CTP system consists of a 9U VME64x chassis with 3 special backplanes and 12 custom designed modules where the functionality is largely implemented in FPGAs. The machine interface module (CTPMI) receives the timing signals from LHC and distributes them over the COM backplane to the other modules. Each of the 3 input modules (CTPIN) receives up to 124 trigger input signals, synchronizes and aligns them and sends them over the PIT bus backplane to the monitoring and core modules. The monitoring module (CTPMON) performs bunch-by-bunch monitoring of the PIT bus signals. The core module (CTPCORE) generates the Level-1 accept signal (L1A) according to programmable selection criteria and sends trigger summary information to the Level-2 and DAQ systems through optical link interfaces (S-LINK). The four output modules (CTPOUT) send the trigger and timing signals to the local trigger processors (LTP) of the sub-detector TTC partitions. Finally the calibration modules (CTPCAL) time-multiplexes the calibration request signals received via the CAL backplane and performs level conversion of front-panel NIM input trigger signals.

CTP Core Module (CTPCORE)





The LUT/CAM FPGA (Xilinx XC2VP50) receives the PIT bus signals on the CTPCORE and implements the LUT and CAM for the trigger formation. DDR input registers were added at the input, the clock for latching the PIT signals can be adjusted using a programmable delay line (CERN DELAY25 ASIC).

Since there are now twice as many trigger inputs, the structure of the LUT and CAM also needed to adapted. An array of 12x16 LUTs generates 448 trigger conditions from the 320 trigger inputs. This includes the internally generated triggers, namely two random triggers, two pre-scaled clocks and eight triggers for programmable groups of bunch crossings. The width of the ternary CAM was also increased from 256 originally to 448 to accommodate all the trigger conditions. However the number of trigger items was kept at 256, because of limited FPGA resources and PCB connections.

The trigger inputs on the CTPCORE are also sent to another FPGA which implements monitoring counters and writes them into FIFO buffers for DAQ/LVL2 readout and monitoring. This functionality is implemented in an Altera Stratix FPGA (EP1S60). Since are not enough PCB connections for the 320 trigger signals, DDR signaling was also used to transmit these signals to the monitoring/readout FPGA. In addition the number of PIT monitoring counters was doubled (324) and the readout formatting unit needed to be adapted to accommodate the additional PIT bus words in the event format.

CTP Trigger Path

Each of the 3 CTPIN modules receives and aligns the trigger signals from 4 input cables with 31 signals each. The switch matrices then drive a subset of the aligned trigger inputs onto 160 PIT bus lines.

The PIT backplane is a short multi-drop bus which spans 5 VME slots and uses SSTL2 levels with a combined series/parallel termination scheme.

Look-up tables (LUT) at the input of the CTPCORE module generate 256 trigger conditions from the 160 PIT signals and additional internal triggers. A ternary contents-addressable memory (CAM) then calculates 256 trigger items as logical combinations of these trigger conditions. After pre-scaling and veto/dead-time logic, the logical or of these 256 items forms the final L1A signal which is fanned out to the sub-detectors. The memory files for the LUT and CAM of the CTPORE and the configuration files for the switch matrices of the CTPINs are automatically generated from the trigger menu by software.

The design of the CTP has been optimized for low-latency, it takes only 4 bunch crossings (BC) from the trigger signals being received at the CTPIN to the L1A being sent from the CTPOUT.

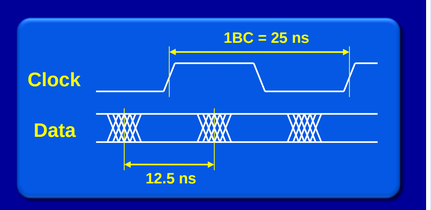
There are a total of up to 372 trigger inputs for the full CTP system, however the number of trigger signals usable in the L1A formation is limited to 160 by the number of PIT bus lines. By operating the PIT bus at 80 MHz using double-data rate (DDR) signaling we manage to double the transfer rate which results in an effective PIT bus width of 320 bits. Although the PIT bus was originally designed to operate at 40MHz, the DDR operation has been shown to work reliably. This modification also required significant changes to the FPGA firmware of the CTPIN, CTPMON and CTPCORE modules.

Testing and Conclusions

Testing

After an extensive verification phase using simulation and timing analysis, the modified FPGA firmware was loaded onto one of the reference CTP systems and tested. Slightly adapted versions of the system test programs from the software framework developed for diagnostics and operation of the CTP were used for this purpose. These test programs allow sending arbitrary data patterns from the test memories on the CTPIN modules and checking the various monitoring counters and FIFOs on the CTPIN, CTPMON and CTPCORE modules.

We also measured the timing window where the PIT bus data could be safely latched by scanning the clock delays on the CTPIN and CTPCORE modules and found good timing margins. The valid data window was 65% (8 ns) of the clock half-period for latching the data at the CTPMON input and 70% (9 ns) at the CTPCORE input. Timing variations between CTPIN modules were small, on the order of 1 ns.



Conclusions

We have presented an upgrade of the ATLAS CTP which increases the number of useable trigger inputs from 160 currently to 320 by operating the PIT bus backplane at 80 MHz using DDR signaling. This was feasible because the PIT bus backplane was carefully designed, and the FPGAs on the CTPIN and CTPCORE modules are still fairly recent and have sufficient spare resources.

The basic functionality of the CTP has been maintained, there are however some limitations:

- The CTPMON can only monitor 160 of the 320 PIT signals due to limited FPGA memory resources and the use of an Altera APEX20KE for the PIT bus interface.
- The mapping of the trigger input signals to the LUT inputs on the CTPCORE using the switch matrices on the CTPIN modules is slightly less flexible since trigger inputs need to be allocated in pairs.
- The latency has increased from 4 to 7 BC (although it may be possible to reduce this to 6 BC).

The CTP upgrade presented here may even be of interest before the LHC luminosity upgrade, since already now all 160 PIT bus signals are allocated, so there is no headroom for potential additional trigger inputs.

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