Contribution ID: **110** Type: **Poster**

# Hardware studies for the upgrade of the ATLAS Central Trigger Processor

*Thursday, 24 September 2009 16:55 (20 minutes)*

The ATLAS Central Trigger Processor (CTP) is the final stage of the first level trigger system which reduces the collision rate of 40 MHz to a level-1 event rate of 75 kHz. The CTP makes the Level-1 trigger decision based on multiplicity values of various transverse-momentum thresholds received from the calorimeter and muon trigger sub-systems using programmable selection criteria. In order to improve the rejection rate for the first phase of the planned luminosity upgrade of the LHC to 3 x 1034 cm-2 s-1, one of the options being studied consists of adding a topological trigger processor, using Region-Of-Interest information from the calorimeter and potentially also the muon trigger. This will also require an upgrade of the CTP in order to accommodate the additional trigger inputs.
The current CTP system consists of a 9U VME64x crate with 12 custom designed modules where the functionality is largely implemented in FPGAs. The constraint for the upgrade study was to reuse the existing hardware as much as possible while not exceeding the latency envelope of 100 ns by a significant amount. This is achieved by operating the backplane at twice the design frequency and required developing new FPGA firmware for several of the CTP modules. We present the design and performance of the firmware for the input, monitoring and core modules of the CTP as well as results from initial tests of the upgraded system.

**Primary author:** Mr HAAS, Stefan (CERN)

**Co-authors:** Mr MESSINA, Andrea (CERN); Mr SHERMAN, Daniel (CERN); Mr BERGE, David (CERN); Mr LUNDBERG, Johan (CERN); Mr BURDALO, Jonathan (CERN); Mr ELLIS, Nick (CERN); Mr FARTHOUAT, Philippe (CERN); Mr SPIWOKS, Ralf (CERN); Mr MAETTIG, Stefan (CERN); Mr PAULY, Thilo (CERN)

**Presenter:** Mr HAAS, Stefan (CERN)

**Session Classification:** POSTERS SESSION

**Track Classification:** Trigger