Contribution ID: **80** Type: **Poster**

An FPGA-based Emulation of the G-Link Chip-Set for the ATLAS Level-1 Barrel Muon Trigger

Thursday, 24 September 2009 16:55 (20 minutes)

The ATLAS Level-1 barrel muon trigger is built as a synchronous pipeline and includes some high-speed serial links in order to transfer data from the detector to the counting room. The links are based on the GLink chip-set, which transfers data
with a fixed and deterministic latency. Despite its unique timing features, the production discontinued and no compatible off-the-shelf chip-sets are available. The transmission side of the links is buried on-detector and will not be upgraded, however a replacement for the receivers in the counting room in case of failures is needed. We developed a replacement solution for GLink transmitters and receivers, based on the gigabit serial transceivers (GTP) embedded in a Xilinx Virtex5-LXT Field Programmable Gate Array (FPGA). In the LHC experiments, and in general wherever an experiment-wide clock is distributed, our link is able to transmit data with a fixed latency, even after a loss of lock or a power cycle.
We present our architecture, showing the GTP internal configuration and the logic in the FPGA fabric needed for the protocol emulation. We compare the GLink and the GTP transmitter eye-diagrams and we discuss the results of Bit Error Rate (BER) and jitter measurements on hybrid (Glink vs. GTP) and homogeneous (GTP vs. GTP) links.

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Session Classification: POSTERS SESSION

Track Classification: Optoelectronics and Links