Integrated Trigger and Data Acquisition system for the NA62 experiment at CERN

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Abstract

The main goal of the NA62 experiment is to measure the branching ratio of the $K^+ \to \pi^+\nu\overline{\nu}$ decay, collecting O(100) events in two years of data taking. Efficient online selection of interesting events and loss-less readout at high rate will be key issues for such experiment. An integrated trigger and data acquisition system has been designed. Only the very first trigger stage will be implemented in hardware, in order to reduce the total rate for the software levels on PC farms. Readout uniformity among different subdetectors and scalability were taken into account in the architecture design.

I. Introduction

The NA62 experiment at the CERN SPS aims at measuring O(100) $K^+ \to \pi^+\nu\overline{\nu}$ events in two years of data taking. The theoretical cleanness of the Standard Model (SM) branching ratio (BR) predictions for this decay mode makes it very attractive both as a powerful test of the CKM paradigm and as a probe for new physics beyond the SM. Experimentally, the detection of this process is very difficult due to the smallness of the signal (in the SM the expected BR is at level of 0.85×10^{-10}) and the presence of a very sizeable concurrent background, mainly from $K^+ \to \pi^+\pi^o$ decays. The present measurement of this decay channel is based on 7 candidates collected by E949 and E787 Brookhaven experiments[1] leading to a value of $BR = (1.47^{+1.30}_{-0.89}) \times 10^{-10}$.

NA62 is a fixed target experiment in which beam of positively charged hadrons, including a fraction of $\sim 6\%$ of kaons, will be produced from 400 GeV/c primary protons from the SPS accelerator. Kaon decays in flight will be observed in a fiducial region ~ 100m long, in vacuum.

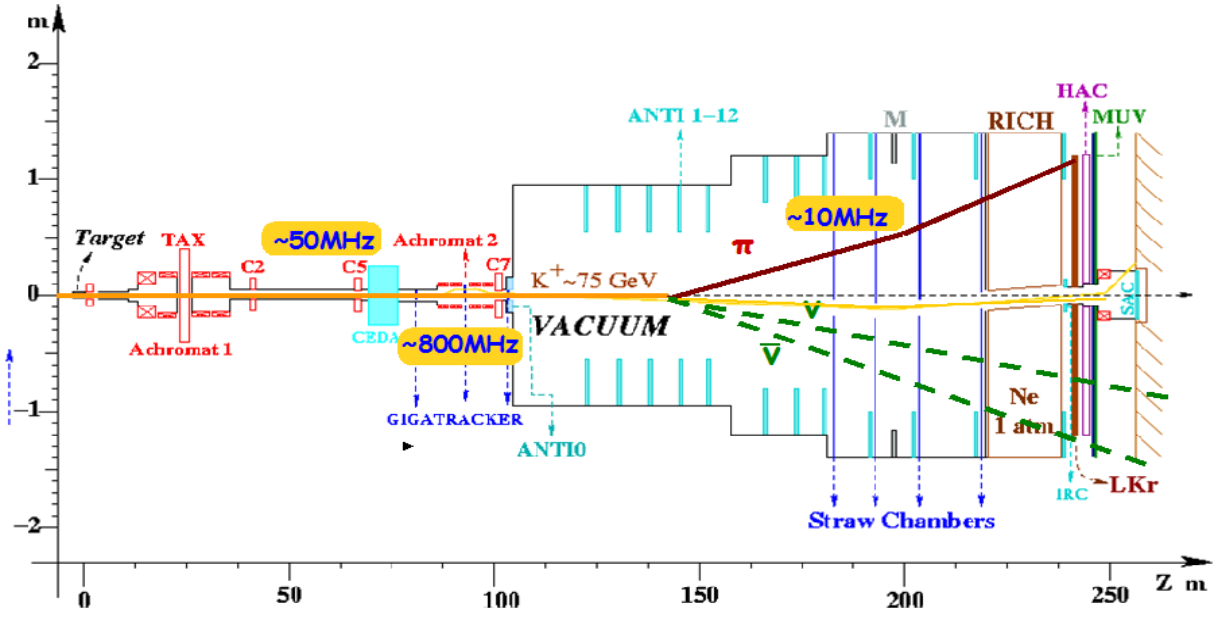

Figure 1: NA62 layout

Decay products and primary particles will be measured by spectrometers, respectively exploiting straw chambers (STRAWS) and silicon pixel detectors (GIGATRACKER), in order to achieve high resolution momenta and angles measurement and consequently good rejection of kinematically constrained background. An efficient veto system for photons and charged particles (LAV, LKr and SAC) and the PID system for primary particles and decay products (CEDAR, RICH and MUV), will guarantee the identification of decay modes not kinematically constrained. In fig.1 the layout of the experiment is shown.

In order to collect the required number of events in a reasonable amount of time, a very intense hadron beam will be employed (3×10^{12} protons per SPS pulse will produce 5×10^{12} K^+ per year). An efficient on-line selection of candidates represents a very important item for this experiment, because of the large reduction to be applied on data before tape recording. On the other hand a loss-less data acquisition system is mandatory to avoid adding artificial detector inefficiencies, e.g. when vetoing background particles. This paper will focus on the general architecture of the integrated DAQ and trigger system for the NA62 experiment.

A. Requests to DAQ and Trigger System

The rate of events in the decay region is strongly dominated by background. According to simulations the rate on the main detectors is around $10MHz$ (table1).

Table 1: Rates on principal detectors

Detector	Rate (MHz)
CEDAR	50
GTK	800
LAV	9.5
STRAWS	8
RICH	8.6
LKR	10.5
MUV	9.2
SAC	1.5

An additional rate of at least $1MHz$ of muons coming from the beam production target, must be taken into account. In this environment the requests to the DAQ and trigger systems are:

- Very low DAQ inefficiency ($< 10^{-8}$);
- High trigger efficiency ($> 95\%$);
- Fully monitored systems;
- Readout without zero suppression for candidates;
- Low random veto probability at trigger level;
- Scalability in terms of bandwidth;

The first request is uncommon in other DAQ systems, but it's crucial for the NA62 experiment, where the full reconstruction of the background is an important issue. For the same reason zero suppression, mainly in the veto detectors, must be avoided as much as possible during the acquisition process. A good trigger efficiency can be obtained using information coming from several detectors with an excellent time resolution, in order to reduce the random veto probability. The final acquisition rate will be of the order of tens of kHz.

B. NA62 trigger and DAQ architecture

A fully digital and integrated DAQ and trigger system has been designed to fulfill the requirements presented in the previous section. The digitization in the early stage of the readout system allows efficient monitoring of each stage of the chain, in order to detect any possible source of losses. The trigger system will be split in two levels: the first stage (L0), implemented in hardware (for instance using FPGAs), will be used to reduce the total rate to $\sim 1MHz$, while the second and third stages (L1 and L2) will be completely software based exploiting powerful PC-farms with large input bandwidth. The data accepted by the L2 will be directly transmitted to the EB (event builder) PC-farm, to be permanently recorded.

The factor ~ 10 in rate reduction at the first stage, will be obtained by a L0 trigger processor (L0TS) using information coming from RICH, LAV, LKr calorimeter and MUV detectors. The trigger primitives from each detector involved in the L0 trigger decision, will be built directly in the same data acquisition board devoted to digitization and monitoring. For all the detectors (apart from GIGATRACKER) the building block of this system will be the TELL1 mother board developed for the LHCb experiment[2].

The TELL1 board (9U format) houses 5 Altera Stratix FPGAs allowing a fully customable configuration. A total RAM memory of 384 MB gives the possibility to store the data in a first buffer stage, waiting for the trigger decision delivered to the board through the TTC[3] interface. A credit card PC (CCPC) allows to control all the functionality of the board. The output stage uses a quad Gigabit Ethernet card (total output bandwidth of $\sim 4Gb/s$). The input stage can be adapted to different purposes using 4 custom daughter boards. On this daughter boards, for instance, the analog data coming from the detector front end could be digitized. The use of uniform system for all the subdetectors allows to have a common fully integrated trigger and readout architecture, exploiting the possibility to use the same data chain to monitor the whole system and avoiding the complications due to independent trigger and readout chains.

C. The TDC board

For the definition of trigger primitives and offline data analysis, several subdetectors will provide the time of arrival of a given events. Time resolution of $O(100ps)$ have to be guaranteed at event rates of $O(10MHz)$ and a good on-line time resolution is also important for the trigger. For this reason we have developed a daughter board (10 layers PCB) for the TELL1 motherboard, providing 128 TDC channels with $100ps$ time resolution. Each mezzanine houses 4 HPTDC chips (developed at CERN[4]) controlled by an Altera Stratix II FPGA used for preprocessing (an on board static RAM memory is also provided for this purpose) and monitoring. Miniaturized connectors are present on both sides of the board, allowing the connection of

128 channels from the subdetectors front-end. Particular care has been used to assure a very good clock stability. The $40MHz$ clock coming from the TELL1 is stabilized by the Stratix II PLL and an external quartz controlled QPLL[5]. After filtering residual noise from DC-DC converters, detailed tests showed that the level of the jitter in the clock is below $40ps$. The intrinsic time resolution of the whole chain for the single hit is measured at level of $50ps$. The time resolution has also been measured in a test beam with a RICH prototype with 400 photomultipliers, and found in agreement with the expectations. A very compact readout system of 512 TDC channels is obtained by mounting four TDC boards on a TELL1. In the TELL1 FPGAs the fine time multiplicity is computed, crucial to define the trigger primitives, by exploiting the high time resolution given by the TDCs. In case the subdetectors need more than one TELL1 for readout the TELL1s will be connected together in a daisy chain using two Gigabit links dedicated to send and receive trigger information.

D. LKr calorimeter readout and trigger

The LKr calorimeter was built for the NA48 experiment[6] to provide excellent energy, time and space resolution. In the NA62 experiment it will be mainly used as veto counter for forward photons from the decay region, but still we want to profit from the good performance of the calorimeter both for background studies and for adding other interesting physics cases to the NA62 main program. Thus LKr calorimeter electronics will provide both time and pulse-height information. An effective approach, already used in NA48, is to perform a continuous sampling with flash ADCs instead of using two separated time and charge measurement. The LKr is composed by $\sim$ 13500 channels sampled at $40MHz$ with an effective resolution of 14 bits. No zero suppression applied at the L0 trigger rate of $1MHz$, would require a $\sim 1TBs$ bandwidth, which the existing NA48 LKr readout cannot stand. The system has thus been modified in order to exploit large buffers (0.5 GB DDR2 per channel) and faster links. The old CPD boards, used to digitize and compute analog sums of groups of cells for trigger purposes, will be reused in $\sim$ 200 "CARE" modules connected with $\sim$ 900 Gigabit links to a readout farm ($\sim$ 200 processor nodes). The 892 analog sums for the trigger (groups of 8x2 cells) will be sent to a system of 28 TELL1 boards housing 32 channels of ADCs each, to provide the first layer of the calorimetric trigger. A second layer of 3 TELL1 boards equipped with Gigabit mezzanine receivers (under design) will produce the LKr trigger primitives for the L0 central processor.

E. L0 central processor

The L0 central processor or L0 trigger supervisor (L0TS) will collect the information from all the detectors participating to the L0 trigger and take the final decision. Montecarlo simulations showed that a factor 10 in rate reduction can be obtained using RICH, LAV, LKr and MUV information. The trigger decision will be dispatched synchronously to the TELL1 boards and other readout systems trough TTC. Two solutions are under investigation to realize the L0TS:

- exploiting parallel processing by Graphics Processing Units (GPU) on a real-time linux High Performance PC with fast I/O connections;
- Custom dedicated board with FPGAs and fast I/O connections;

The first solution is limited by the request to take decisions with a stable latency of one ms, depending on the front end buffer size in some critical detectors. The possibility to have such a latency, given by the large buffers in the TELL1, will be exploited to compensate the ethernet intrinsic latency and the computing time in the GPU-HPPC's solution.

F. L1 and L2 levels

The L1 trigger will be totally software. For each subdetector a dedicated PC (or a small cluster of PCs) will be used to implement fast reconstruction to apply single subdetector standalone algorithms (clusters presence in the LKr, tracks direction and momentum in the STRAWS, etc.). The input event rate for these PCs will be $1MHz$. The data will arrive at the L2 PC farm through a commercial GBE switch. At this level the full event will be completely reconstructed and more sophisticated high level trigger algorithms will be implemented, with the request of reduction at total rate of tens kHz for permanent recording on tape. Assuming a single event size of $10kB$ (heavily dominated by LKr and GIGATRACKER) the total bandwidth at the end of the chain will be of the order of $100MB/s$ to be recorded.

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