Contribution ID: **81** Type: **Oral**

Integrated Trigger and Data Acquisition system for the NA62 experiment at CERN

Wednesday, 23 September 2009 09:45 (25 minutes)

The TDC based integrated trigger and data acquisition system of the NA62 experiment at CERN will be presented. The system architecture, the trigger algorithm and its implementation in commercial high performance FPGAs will be described. The results of test and characterization of the custom components as well as those of extensive field tests performed on a system prototype handling up to 512 input channels will be discussed.

Summary

The NA62 experiment at CERN (SPS) will measure the ultra rare Kaon decay to one Pion and two Neutrinos using detectors with sub-nanosecond resolution. Relevant events will be triggered when a minimum amount of hits in time coincidence is detected in the active detectors (e.g.: the RICH) with no hits in others ("vetoes").

The Trigger and DAQ system is based on components designed for the LHC experiments. The building blocks are the High Performance Time to Digital Converter (HPTDC), designed at CERN, which can measure the timing of rising and falling edges ("hits") on 32 input signals with a resolution of 100ps and the TELL1, a general-purpose data acquisition board developed for the LHC-b experiment.

We developed a custom mezzanine board (TDCB) housing 4 HPTDCs; 4 such boards can be plugged on one TELL1 resulting in 512 input channels handled in one VME-9U board.

Each TELL1 is equipped with 4 FPGAs (PP) that handle the readout of the TDCB and the storage of raw data in memory buffers while waiting for the global trigger and implement the trigger algorithm counting hits in time slots of a few nanoseconds. A fifth FPGA (SYNCLINK) combines the outputs of the PP FPGAs and handles the formatting and transmission of trigger and raw data through 4x1Gb Ethernet ports.

TELL1 boards can be daisy-chained and in each SYNCLINK FPGA the local trigger data is combined with that evaluated by the previous element of the chain and transmitted to the next. 2 Ethernet ports are used for this purpose and the other two handle the raw data transfer to PCs.

An embedded processor controls all the devices in the TELL1 and in the TDCBs through JTAG and I2C links. The clock is handled by a TTC-RX device and the clock jitter is reduced by QPLL devices to less than 50ps not to affect the HPTDC time measurements.

The TDCB is equipped with an Altera Stratix II device that handles the configuration of the HPTDCs through a dedicated JTAG port and controls the QPLL. The HPTDC readout can be directly controlled by the PP FPGAs if no data pre-processing is performed in the TDCB FPGA or it can be handled by TDC controllers embedded in the TDCB FPGA if raw data are locally pre-processed (e.g.: timing re-ordering is performed), stored in a local memory buffer and directly accessed by the PP FPGAs. Monitor functions as embedded TDC emulators, hit and error counters, detection of QPLL unlock condition and TDC calibration with external pulses are also handled by the TDCB FPGA.

The TDCB has been fully tested and characterized and results will be shown in this paper. The architecture of the board and the features embedded in the TDCB FPGA will be described in detail as well as the general architecture of the Trigger and DAQ system. Results of the test performed on a prototype of the entire system including a 440 channel detector, Front-End electronics and one fully equipped TELL1 will be also presented.

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Session Classification: Parallel Session A3 - Trigger

Track Classification: Trigger