Contribution ID: **86** Type: **Oral**

Performance of the ABCN-25 readout chip for ATLAS Inner Detector Upgrade

Tuesday 22 September 2009 11:25 (25 minutes)

We present the test results of the ABCN-25 front end chip implemented in CMOS 0.25um technology and optimized for the short, 2.5cm, silicon strips intended to be used in the upgrade of the ATLAS Inner Detector. We obtain the full functionality of the readout part, the expected performance of the analogue front-end and the operation of the power control circuits. The performance is evaluated in view of the minimization of the power consumption, as the upgrade detector may contain up to 70 millions channels. System tests with different power distribution schemes proposed for the future tracker detectors are possible with this chip. The ABCN-25 ASIC is now serving as the prototype readout chip in the developments of the modules and staves for the upgrade of the ATLAS Inner Detector.

Summary

An important component of the development program of silicon strips tracking system for the upgrade of the ATLAS experiment at the S-LHC is the ABCN-25 front-end readout chip. The ABCN-25 chip is designed for binary readout of silicon strip detectors. The design follows the architecture of the ABCD3T design implemented in BiCMOS DMILL technology and used in present ATLAS SCT detector. The primary goal of the ABCN-25 chip is to provide a test vehicle for the detector module development program and at the same time optimization of the front-end power consumption, for short strips of 2.5cm, with an ENC noise below 800 electrons. The other target is the development of a full digital readout chain, with 6.2us trigger latency, zero suppression, and a serial readout protocol compatible with the actual readout systems but able to run at higher speed (80Mb/s). The chip incorporates two current shunt devices, to evaluate the serial power distribution, and a voltage regulator for the analogue frontend, compatible with both the serial power and the DC-DC power systems.

The ABCN-25 chips have been fabricated with the IBM CMOS6 technology and full functionality has been demonstrated. The performance of the chip has been measured both for the analogue and digital functions by using a dedicated "one-chip"test board. The performance of the front-end circuit optimized for short strips are measured for different bias conditions and load capacitances. Noise measurements on preliminary hybrid boards with 20 ABCN-25 connected to a silicon strip detector will be shown for comparison. For the nominal power consumption of 0.7mW in the front-end, the measured ENC for 2.5pF detector capacitance is below 800e-. Time walk and linearity are also measured to compare the performance with numbers expected from simulation.
The functionality of the digital part of ABCN-25 has been fully verified. The daisy-chain readout of up to 10 chips at the speed of 80Mb/s has been proven. As the power consumption of the digital part is becoming dominant, the power consumptions of the different functional blocks of the chips (namely the pipeline, the readout system and the command decoder) are measured and discussed. The average digital current of 130mA at 2.5V is around 30% higher than the initial estimation. The excess current is partially due to the final optimization of the digital block design, as the final design tool optimizers are efficient in favoring the timing performance, but at the cost of additional clock buffers. The estimation of the power consumption with the ABCN-25 architecture but with a 130nm technology, and the possibilities of power reduction by design, will be discussed.
One of the two on-chip shunt circuits is made of a large current shunt device. The control with feedback of this device is through a filtered input to its gate. The second on-chip shunt circuit is stand-alone on chip and contains a novel control circuit, which ensures uniform distribution of the shunt current in many shunt regulators (up to 20) connected in parallel on the module as required for the serial powering system. A dedicated "4-chips"test board for the evaluation of these circuits has been made and test results with the two shunt circuits will be shown. The potential limitations of these devices in the foreseen implementation of 20 ABCN-25 chips powered in parallel on one hybrid board will be discussed.

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Session Classification: Parallel session A1 - ASICs

Track Classification: ASIC's