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Advanced Pixel Architectures for Scientific Image Sensors

Tuesday, 22 September 2009 11:00 (25 minutes)

We will present recent developments from two projects targeting advanced pixel architectures for scientific applications. Results will be reported from test structures demonstrating variants on a 4T pixel architecture. The variants include differences in pixel and diode size, the in-pixel source follower transistor size and the capacitance of the readout node to optimise for low noise and high dynamic range. Results will also be reported from TPAC, a complex pixel architecture, which has been manufactured with a special deep P-well process and on a high resistivity substrate for enhanced charge collection performance.

Summary

The scientific community often requires advanced sensors which are able to detect small amounts of charge. The requirements can include high sensitivity, low noise, high charge collection efficiency and a tolerance to radiation. To achieve these requirements, we are developing advanced pixel architectures, two of which are presented in this paper: 4 transistor (4T) pixels and complex pixels with full in-pixel CMOS circuitry. In both cases, we are also exploring high resistivity substrates to improve the charge collection efficiency.

In a standard substrate material, charge arising from an incident photon/particle moves by diffusion, and is collected only when it reaches the depletion region around the collecting diode (typically 1-2μm). High resistivity substrates can provide full depletion of the sensing layer, and the extended electric field improves charge collection time and efficiency. Alongside this, a deep P-well implant, developed by us in conjunction with a leading CMOS image sensor foundry, allows advanced circuitry to be implemented inside pixels without a detrimental effect to the charge collection.

The FORTIS (4T Test Image Sensor) project is dedicated to developing test sensors containing a 4T pixel fabricated in a specialised 0.18μm CMOS image sensor technology. The sensors contain thirteen different pixel variants on a 15μm pitch, including differences in the capacitance of the readout node to increase the conversion gain, variations in pixel pitch up to 45μm together with increased diode sizes to improve the charge collection efficiency, and variations in in-pixel source follower transistor size to decrease the noise distribution. The project also investigates the architecture further with the addition of a high resistivity substrate and the deep P-well layer to improve the charge collection efficiency. Two prototypes have been fabricated and results from the first one demonstrate a low noise value of 5.8e- and a conversion gain of 60μV/e- as measured at the sensor output. The second prototype which aims to improve these values further is currently undergoing testing, and the results will be available for the Workshop.

FORTIS sensors are currently undergoing testing for radiation hardness by irradiating with x-rays. The results will give us an insight into how tolerant the 4T pixel architecture is to ionising radiation, and may suggest where the radiation damage occurs to improve future designs.

The TPAC (Tera-Pixel-Active-Calorimeter) sensor was designed to demonstrate digital calorimetry for a silicon tungsten ECAL at the ILC. This device has now been manufactured with a uniform pixel array on standard and high resistivity substrates. The charge collection performance of pixel test structures is evaluated using a pulsed IR laser to demonstrate the improvement achieved by the deep P-well implant and high resistivity substrates. The status of the TPAC project, including latest results on the sensor performance, will be reported.

The results from both sensors are an exciting addition to the field of scientific image sensor development. The architectures and processing variations explored are applicable to a wide range of other applications where low noise readout and high sensitivity to small amounts of charge is required.

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