A flash high-precision Time-to-Digital Converter implemented in FPGA technology

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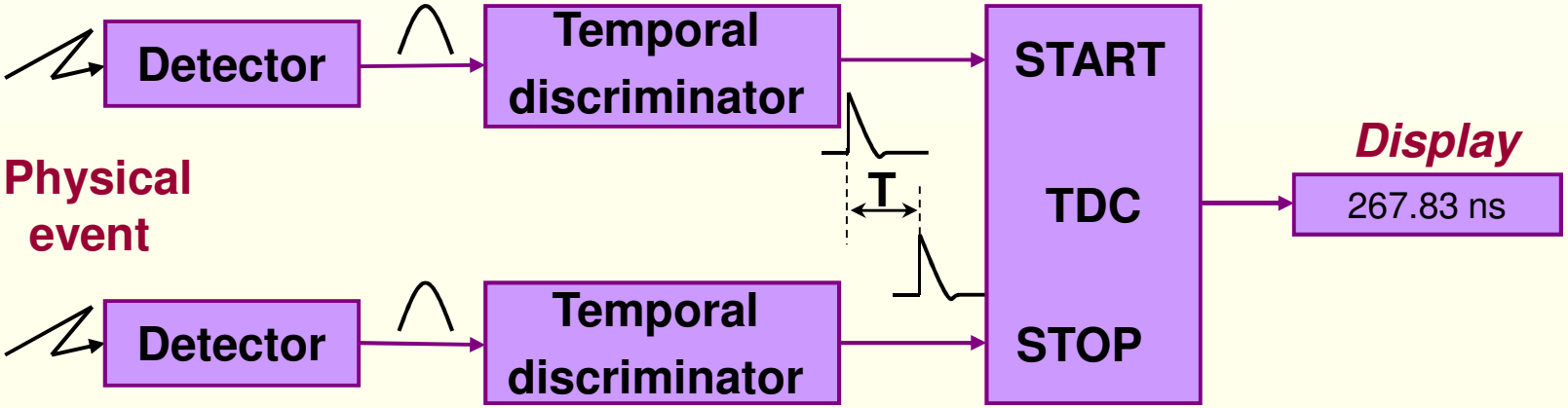
Summary

- ✓ Definition and application of a TDC;
- ✓ TDC's characteristic parameters;
- ✓ FPGA (Field Programmable Gate Array) devices;
- ✓ TDC architectures: fine and coarse structures;
- ✓ TDC Tester Board;
- ✓ Conclusions.

Time interval measurements

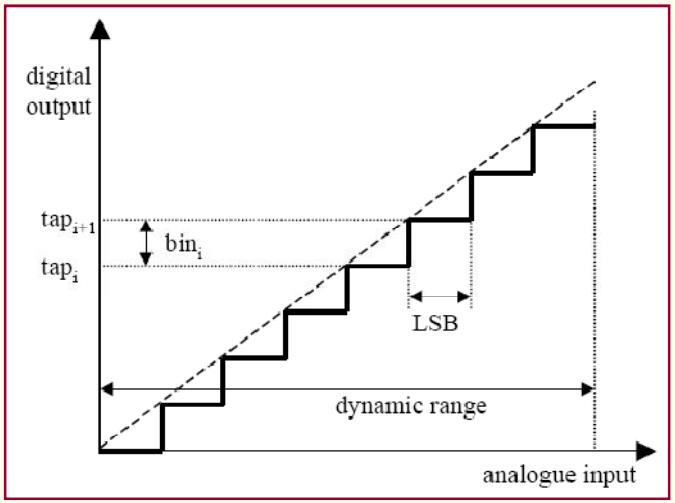


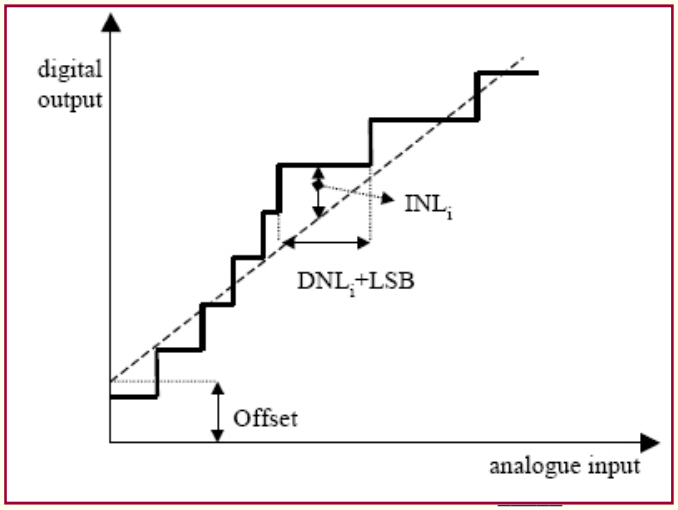
Applications of a TDC in Physics

- ✓ The flight time of particles;
- ✓ The life time of particles;
- ✓ The decay time of scintillators;
- ✓ Laser range finding;
- ✓ Time of flight mass spectrometry;
- ✓ Time of flight Positron Emission Tomography (TOF - PET).

Characteristic parameters of a TDC

- ✓ Dynamic range: the larger delay that can be measured;
- ✓ Resolution: the least value of the measured quantity;
- ✓ Readout speed: how fast the instrument can produce a result;
- ✓ Differential nonlinearity: deviation of the output bin size from its ideal value of one least significant bit (LSB);
- ✓ Integral nonlinearity: deviation of the input/output characteristic and a straight line of ideal gain (slope) that best fits the curve.



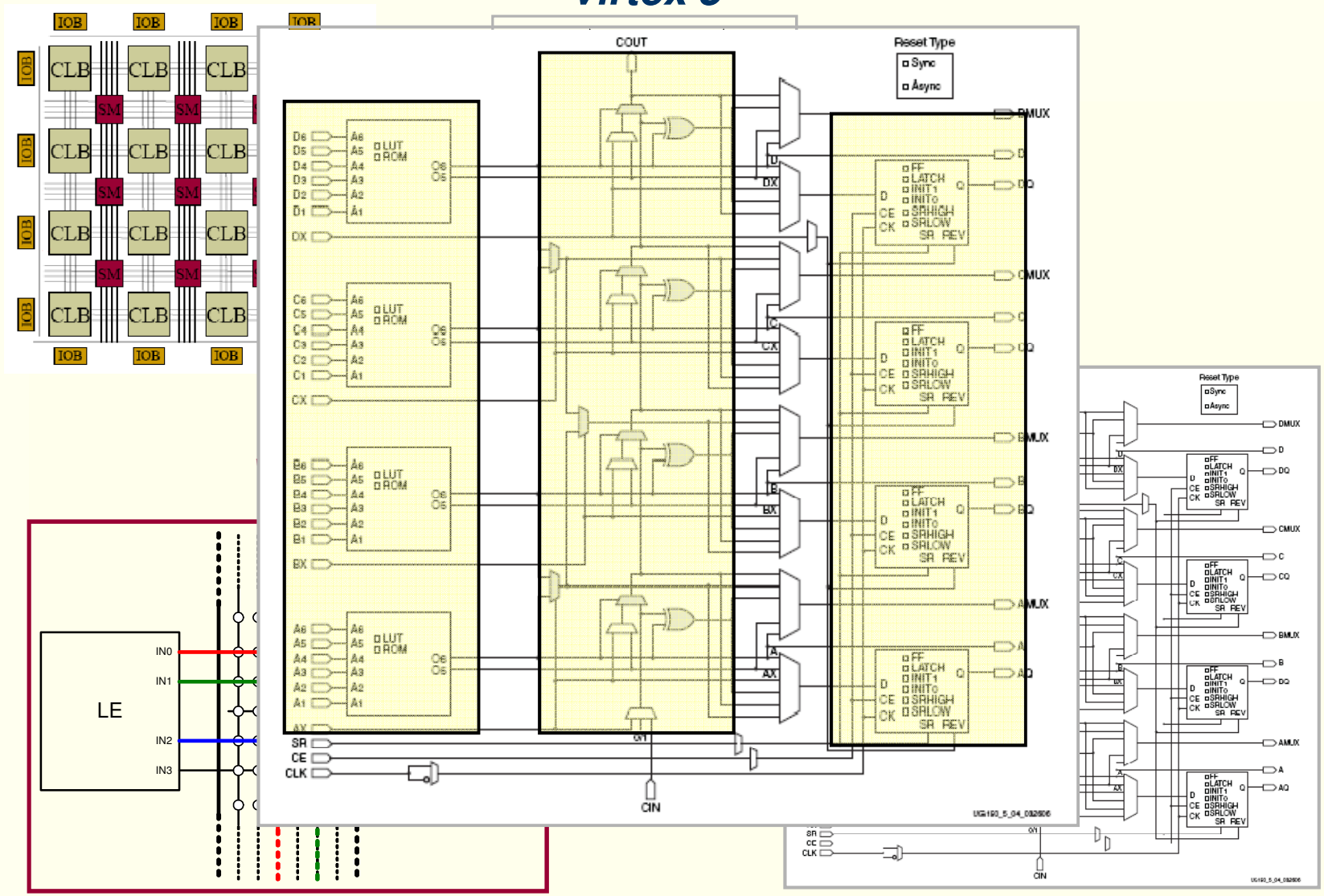


$$DNL_i = \frac{LSB_i - \overline{LSB}}{\overline{LSB}}$$

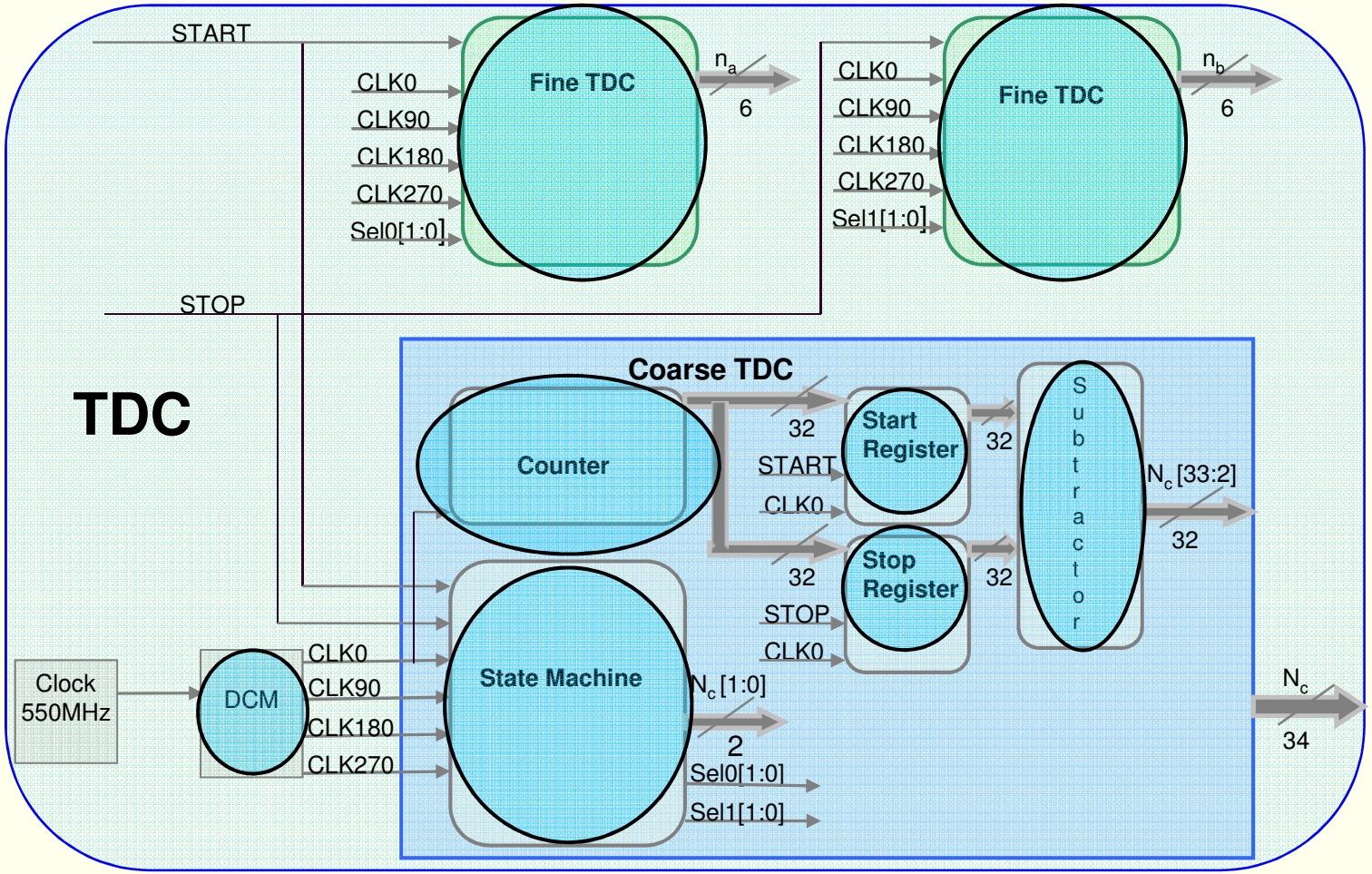
$$INL_j = \sum_{i=1}^{j} \frac{1}{M} \frac{LSB_i - \overline{LSB}}{\overline{LSB}}$$

FPGA structure

Virtex 5

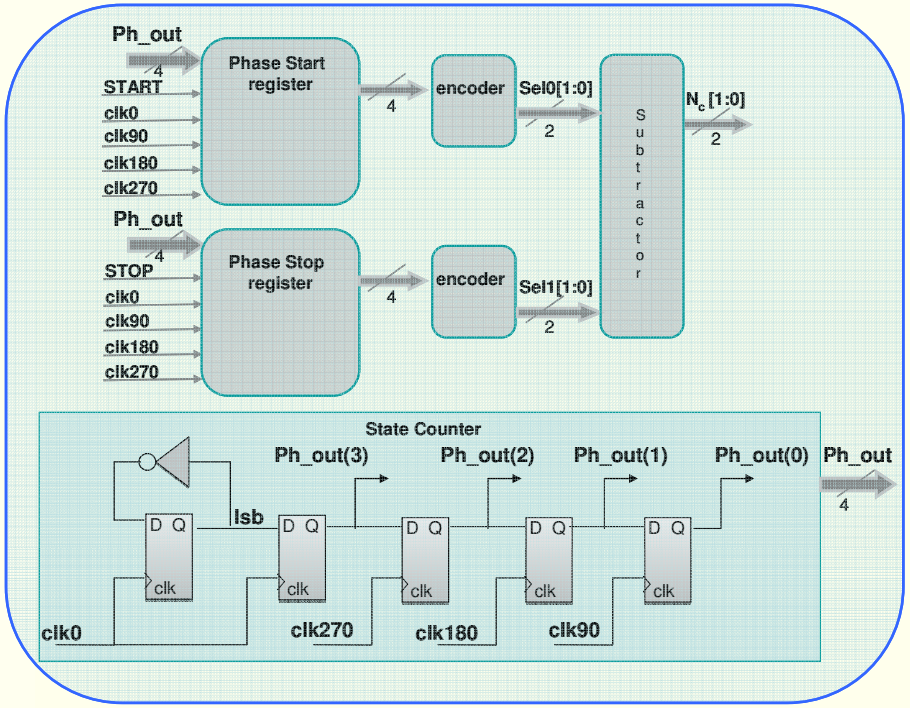


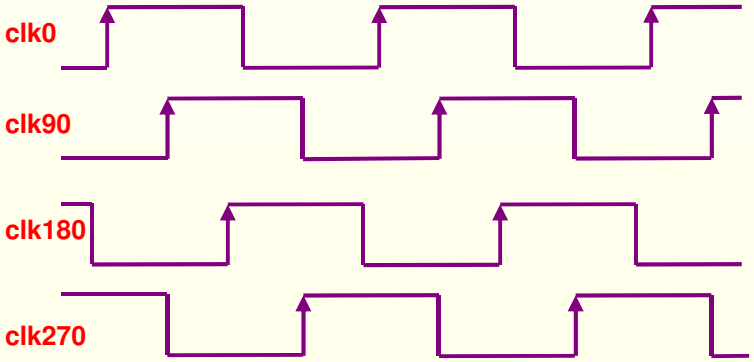
TDC architectures: fine and coarse structures



The counter is used in free-running mode. When the START signal transition occurs, the current state of the counter is sampled by the START register, and the same operation occurs also when the STOP signal is delivered to the TDC. The difference between the STOP and the START register is the coarse measurement of the time interval.

The state machine





The state machine samples the START and the STOP signal and detects the phase difference between the START and STOP rising edges. The least significant bit corresponds to a quarter of the clock period

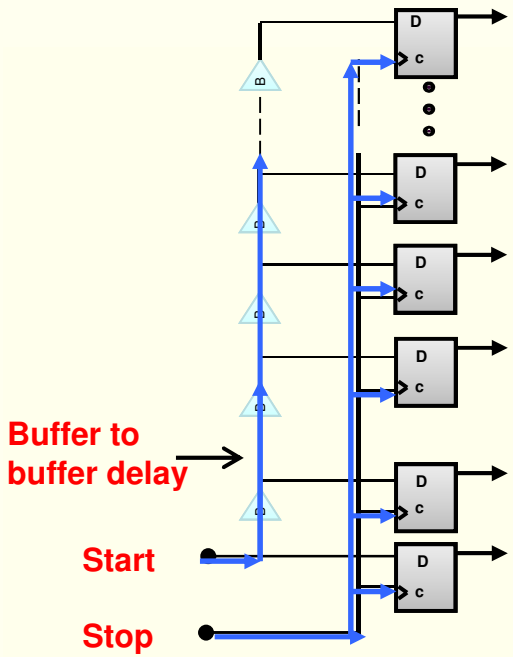
The state counter changes the output every quarter of the clock period.

Ph_out(3)	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Ph_out(2)	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1
Ph_out(1)	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Ph_out(0)	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
Decimal output	10	2	6	4	5	13	9	11	10	2	6	4	5	13	9	11	10	2	6	4	5	13	9	11
Decoded decimal output	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3

Furthermore the state machine is usefull to the delay line selection of the fine TDC performed in the carry chain delay line architecture.

Fine structure(1)

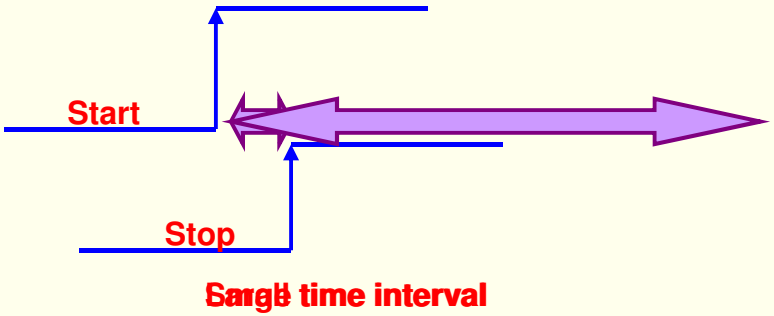
The fine TDC, for the measurement of the short time intervals has been performend using a flash architecture:



$T_{MAX} = N\tau$ ⇐ **Max measurable time**

$T_P = N\tau$ ⇐ **Propagation time of the line**

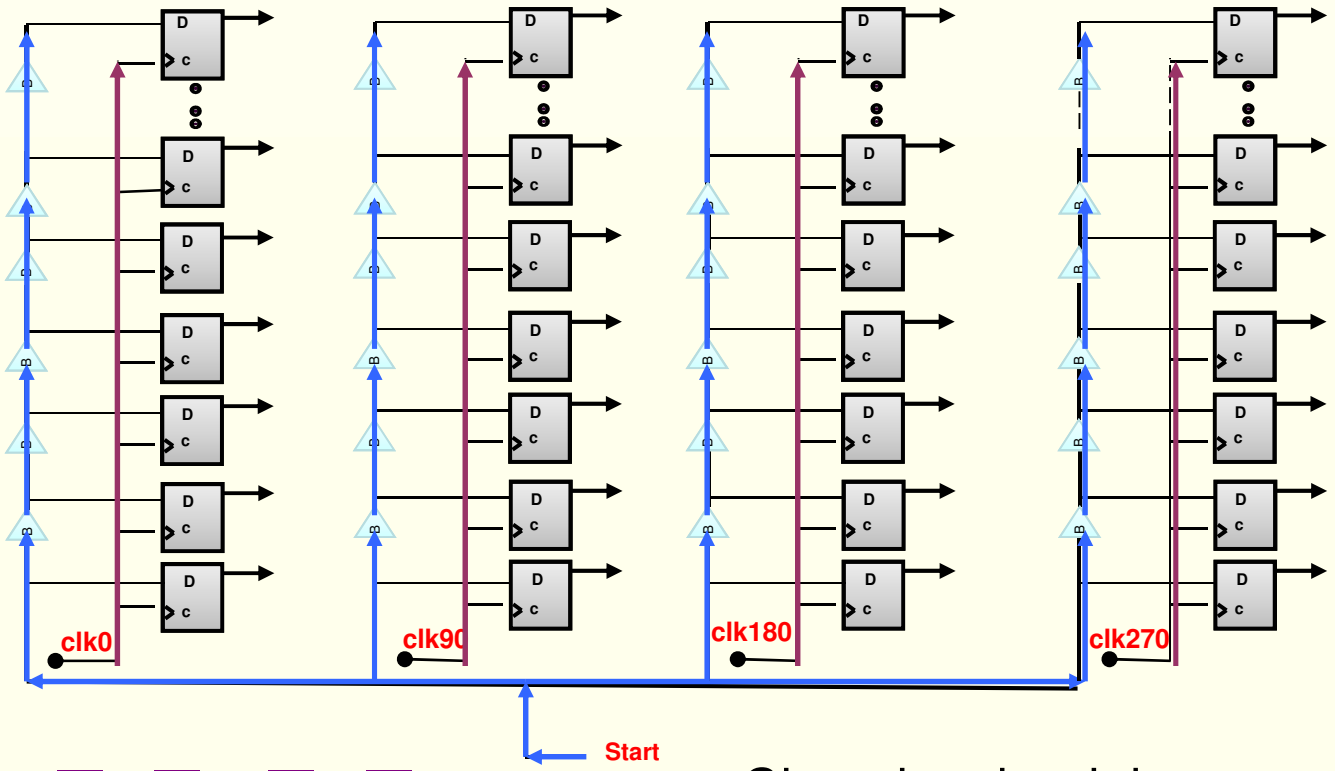
τ ⇐ **Resolution**

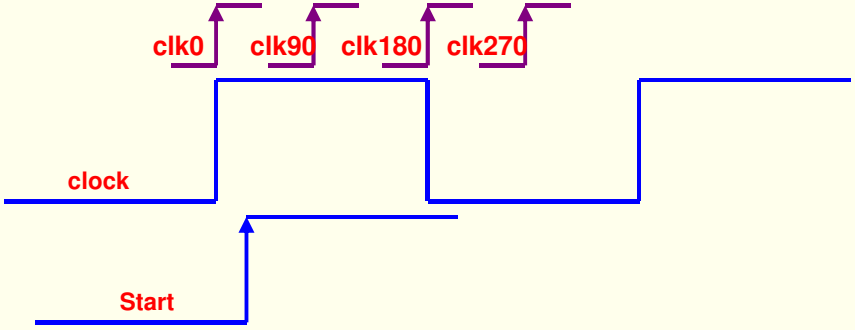


Carry chain delay line

This structure makes use of buffers connected between them by fast lines. The START signal after each delay unit is sampled by pertaining flip-flop on the rising edge of the STOP signal. This structure have a very short dead time equal to one clock period.

Fine structure(2)





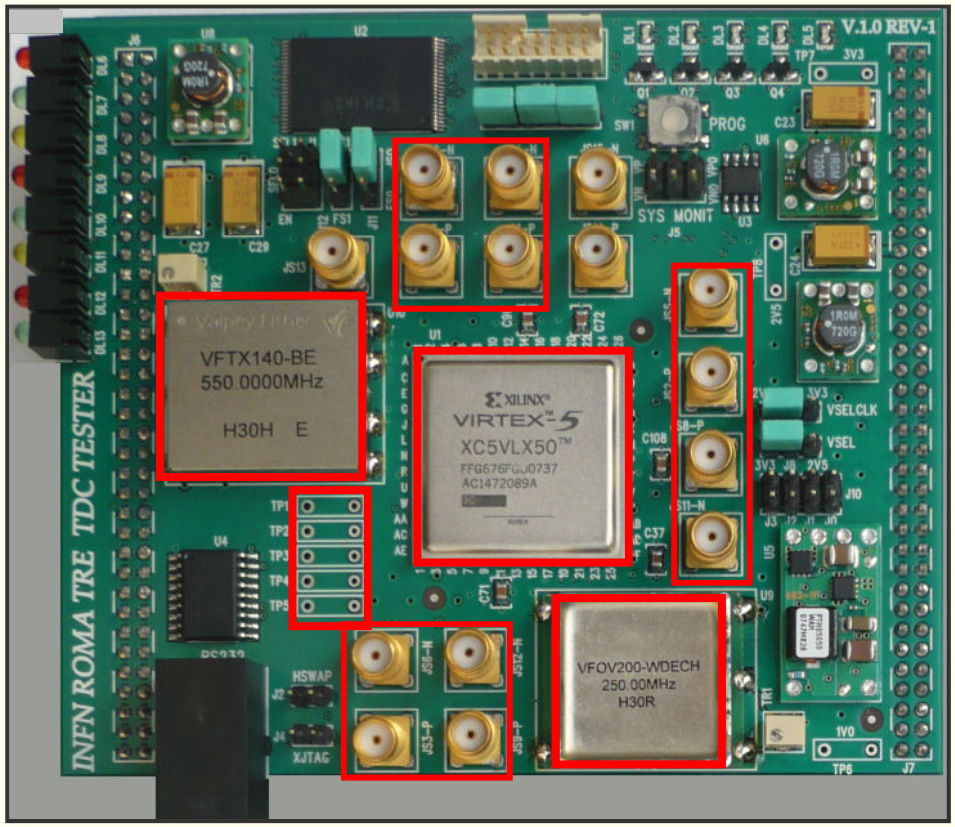
Choosing the right tapped delay lines

The selection of the tapped delay line reflects the phase difference between the Start signal and clk0.

TDC Tester board (1)

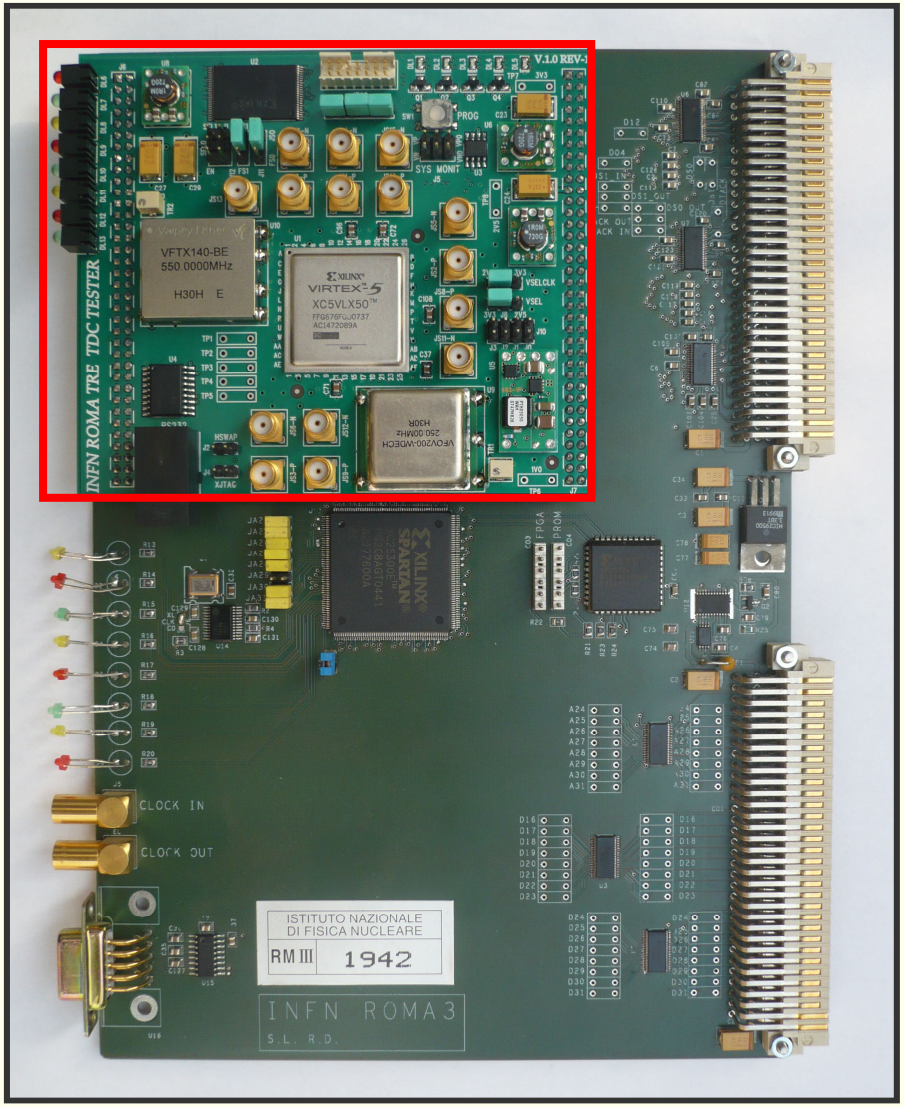
We designed and built a PCB hosting a Virtex 5 FPGA to test the TDC architecture. On the TDC Tester board, two high stability oscillators have been installed in order to compare their performance.

- ✓ The first oscillator generates an output frequency of 550 MHz.



- ✓ The second one provides an output frequency of 250 MHz .
- ✓ Test points for high bandwidth active probes are used to perform the Virtex 5 clock signal characterization. They are placed just near the FPGA, making the shortest distance for the device output signals.
- ✓ SMA connectors are used to send the START and STOP signals to the board. They may adopt differential lines or single ended signaling schemes.

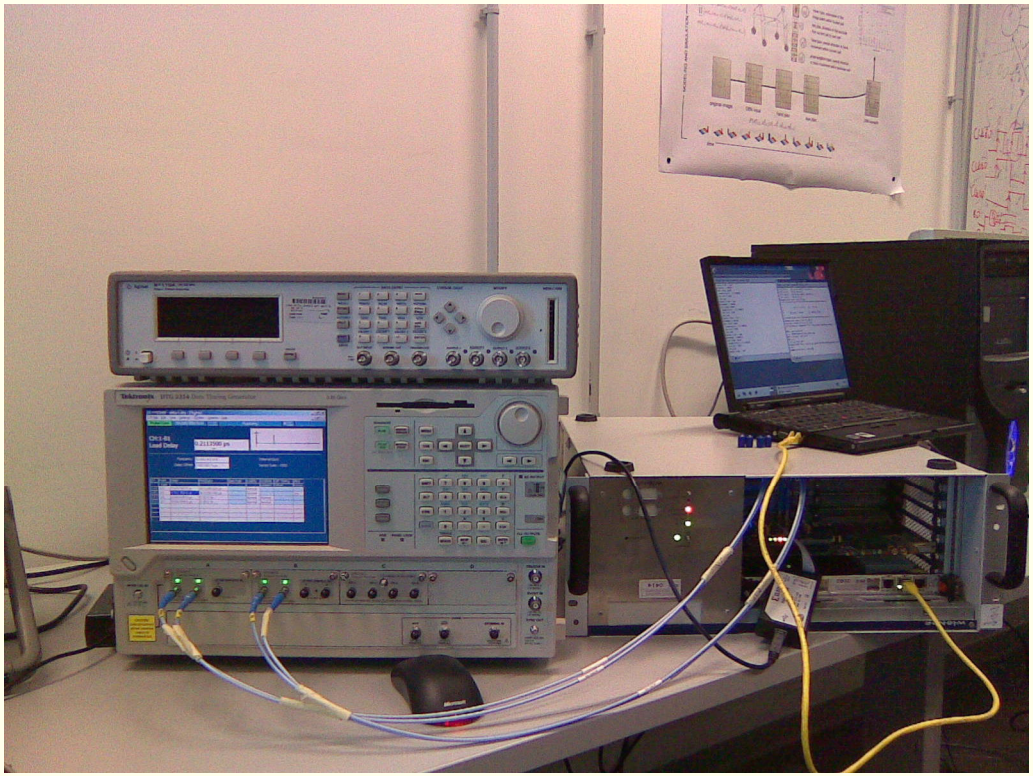
TDC Tester board (2)



The TDC Tester board is hosted by a VME module which allows us to test and read-out the TDC via a CPU Motorola MVME6100.

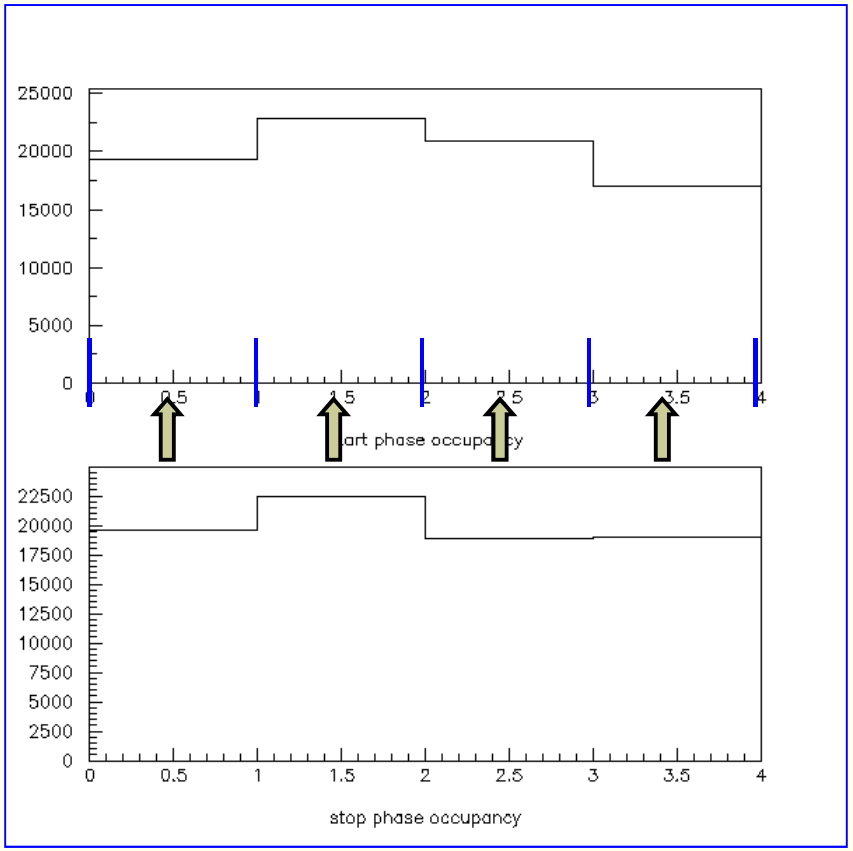
Test set-up

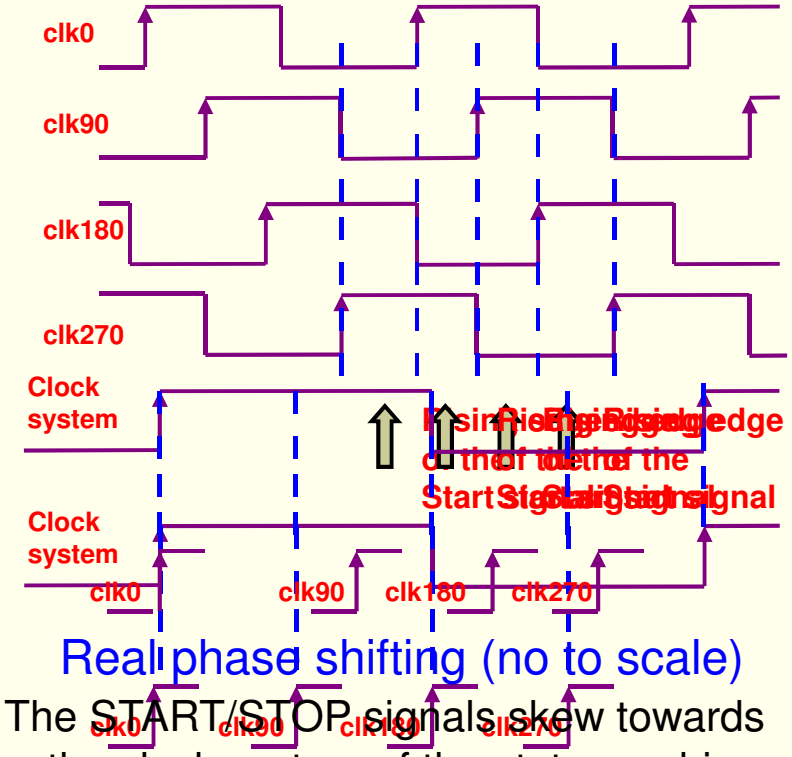
To perform our tests we have used an architecture based on an off-shelf CPU board, the Motorola MVME6100. The VME board hosting the TDC Tester daughter card can handle A32/D16 VME cycles and is configured as slave. We have used a DTG5334 as pulse generator in order to deliver to the TDC time intervals up to 20 us with steps better than 1 ps. Since we have operated the DTGM in free running mode an accept signal was delivered by the MVME6100 to the VME slave board in order to start and stop measurements.



Phase detecting

We executed tests of the phase occupancy of the rising edge of the start and stop signal within the system clock period. The figure below shows a plot of the hit counts as function of the phase value of the clock period for a 100 ns time interval measurements. 80000 measurements were made.





Real phase shifting (no to scale)

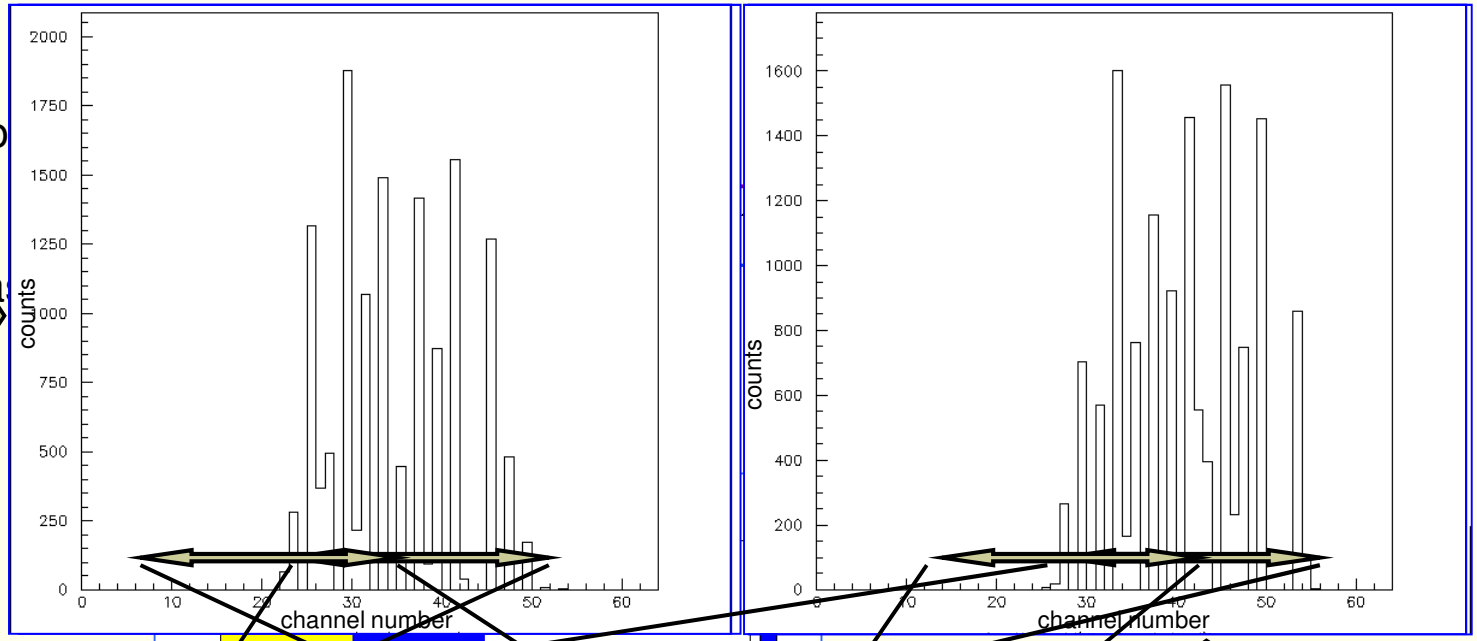
The START/STOP signals skew towards the clock system of the state machine can be simplified as a clock signals deviation from the ideal behavior.

Ideal phase shifting

Phase correlation

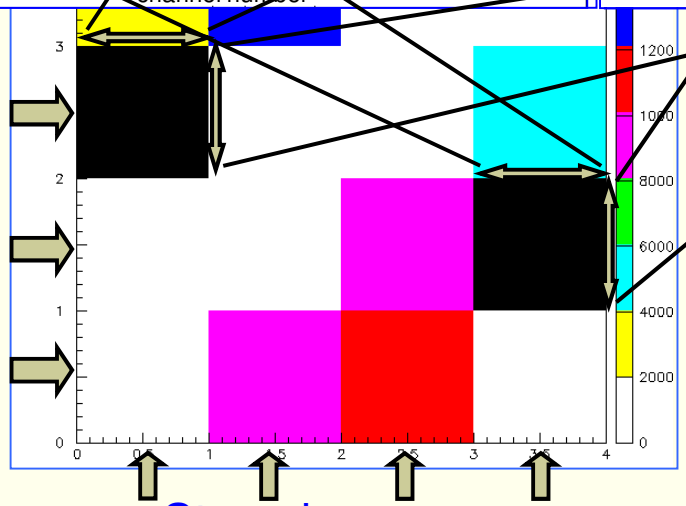
The co
edge
mea

Stop delay line



Start delay line

Start phase measure



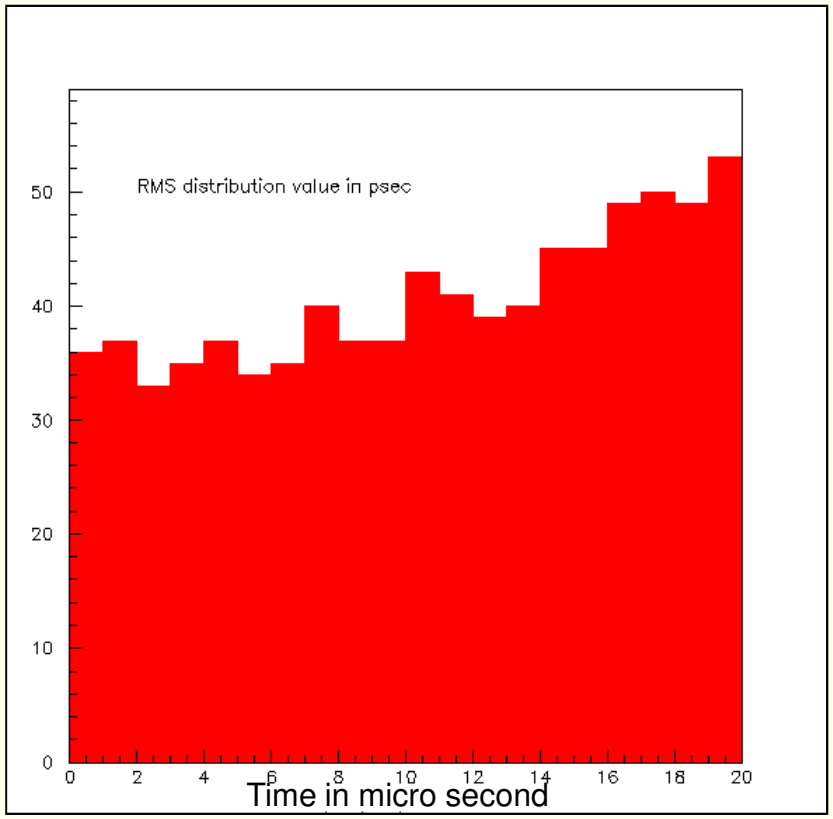
Stop phase measure

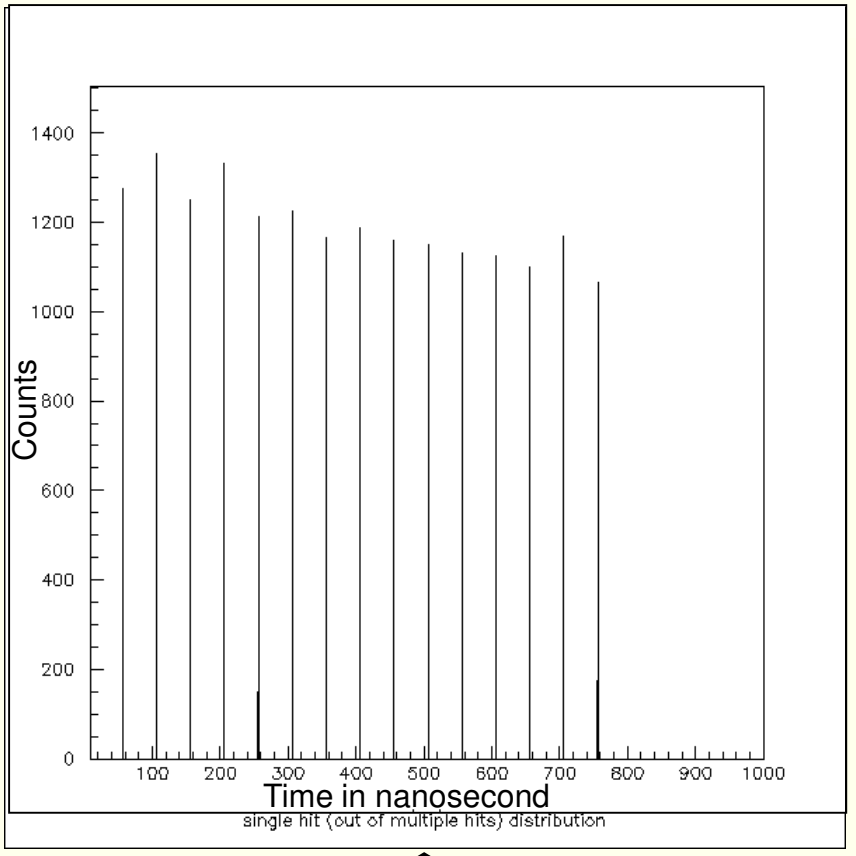
Phase correlation

The plots above are showing the hit counts as function of the channel number for the START/STOP carry chain delay lines

RMS of the measurements

We measured time interval up to 20 us and the rms of the measurements is between 35 ps and 55 ps



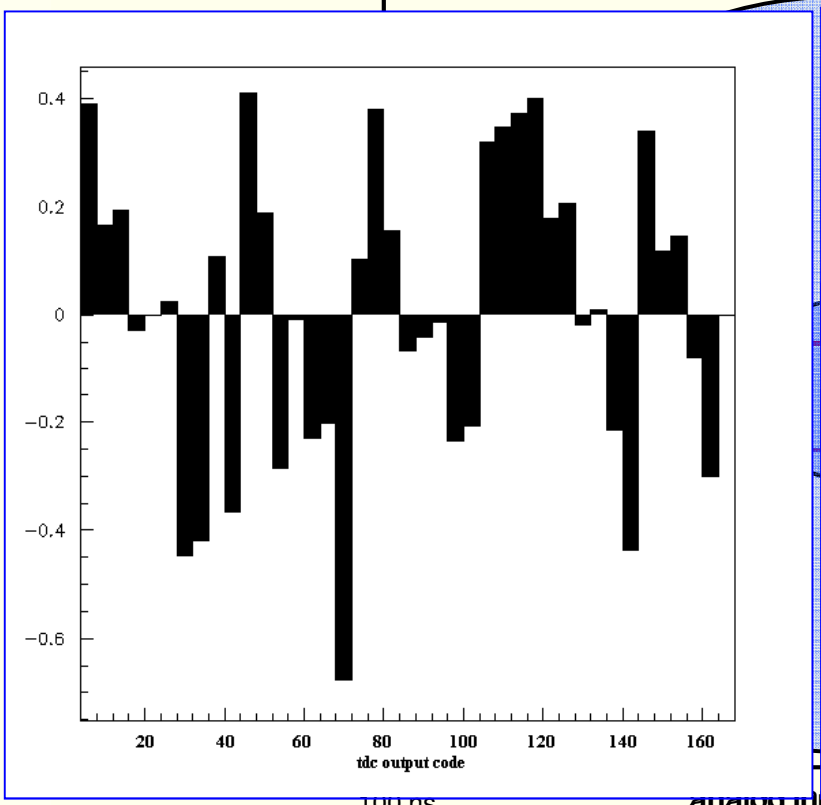


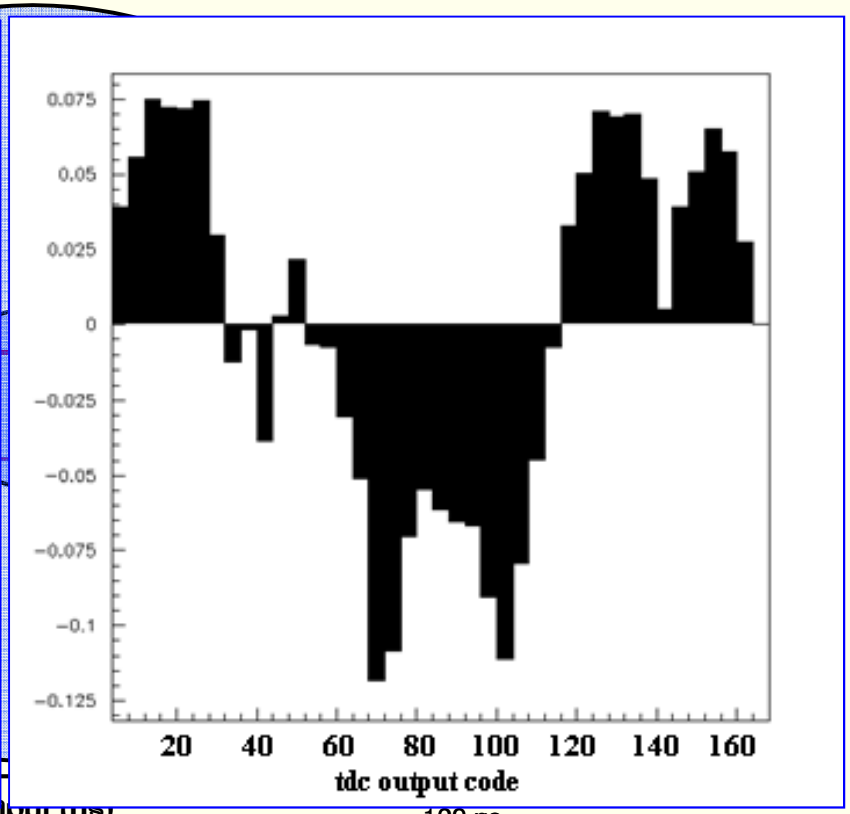
RMS of the time interval measurements

Multi hit measurements

Non linearity of the measurements

The TDC is linear up to 20 us and we measured the integral and differential non linearity within the clock period on a 2 ns time interval from 100 ns to 102 ns as function of the TDC output code.





100 ns

analog input (us)

102 us

$$DNL_i = \frac{LSB_i - \overline{LSB}}{\overline{LSB}}$$

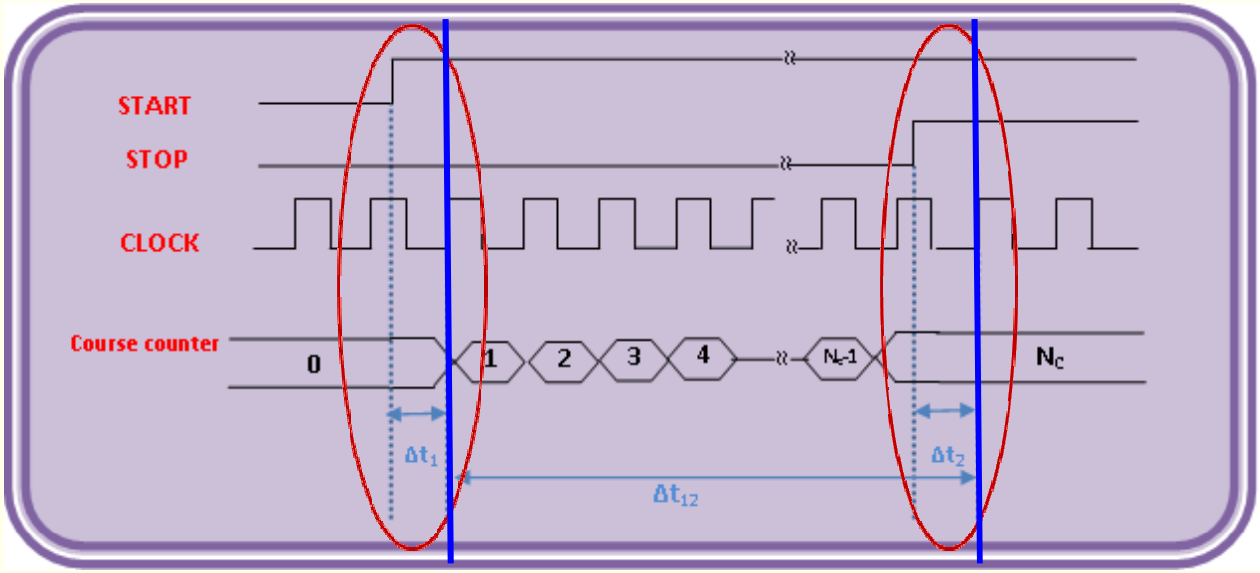
$$INL_j = \sum_{i=1}^{j} \frac{1}{M} \frac{LSB_i - \overline{LSB}}{\overline{LSB}}$$

Conclusions

- We have measured a time resolution of about 50 ps on every single measurement.
- The TDC flash architecture is virtually dead time free.
- FPGA electronics technology offers high design flexibility of the TDC

Back-up slides

Nutt's interpolation



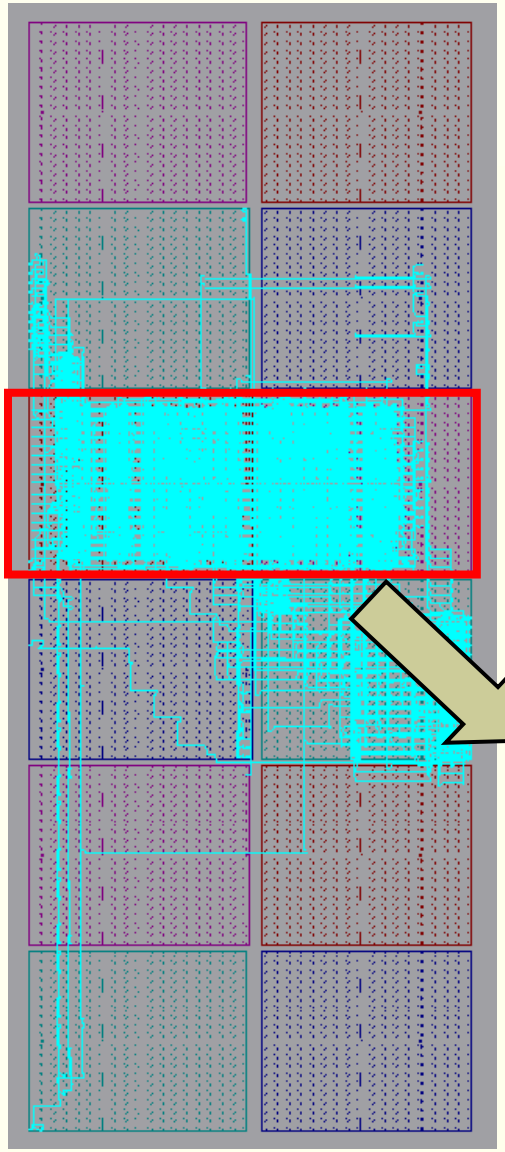
Δt_1 : time interval between the rising edges of the START signal and the next reference clock;

Δt_{12} : time interval between the two rising edges of the reference clock immediately following the rising edges of the START and the STOP signals;

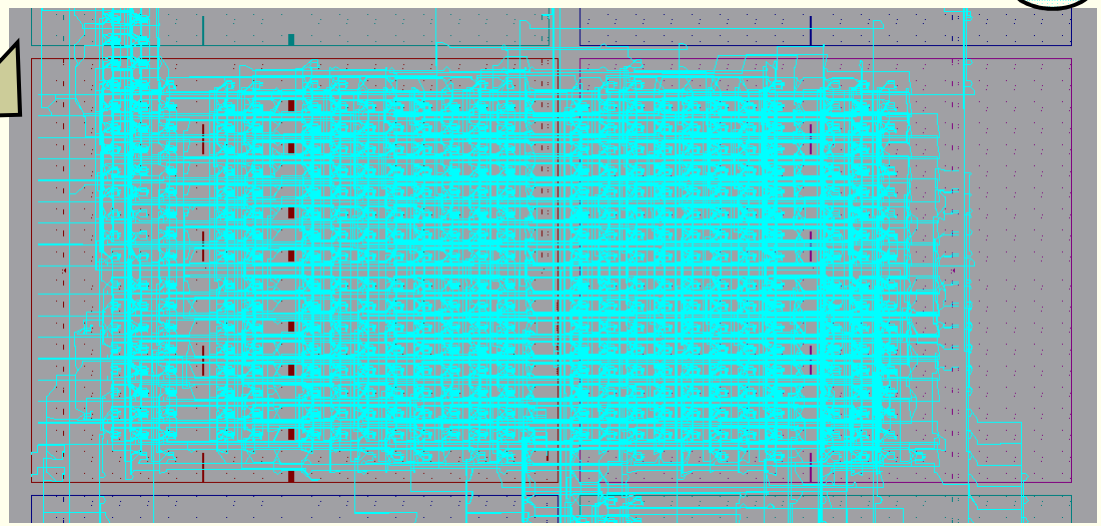
Δt_2 : time interval between the rising edges of the STOP signal and the next reference clock.

$$T = (\Delta t_1 + \Delta t_{12} - \Delta t_2)$$

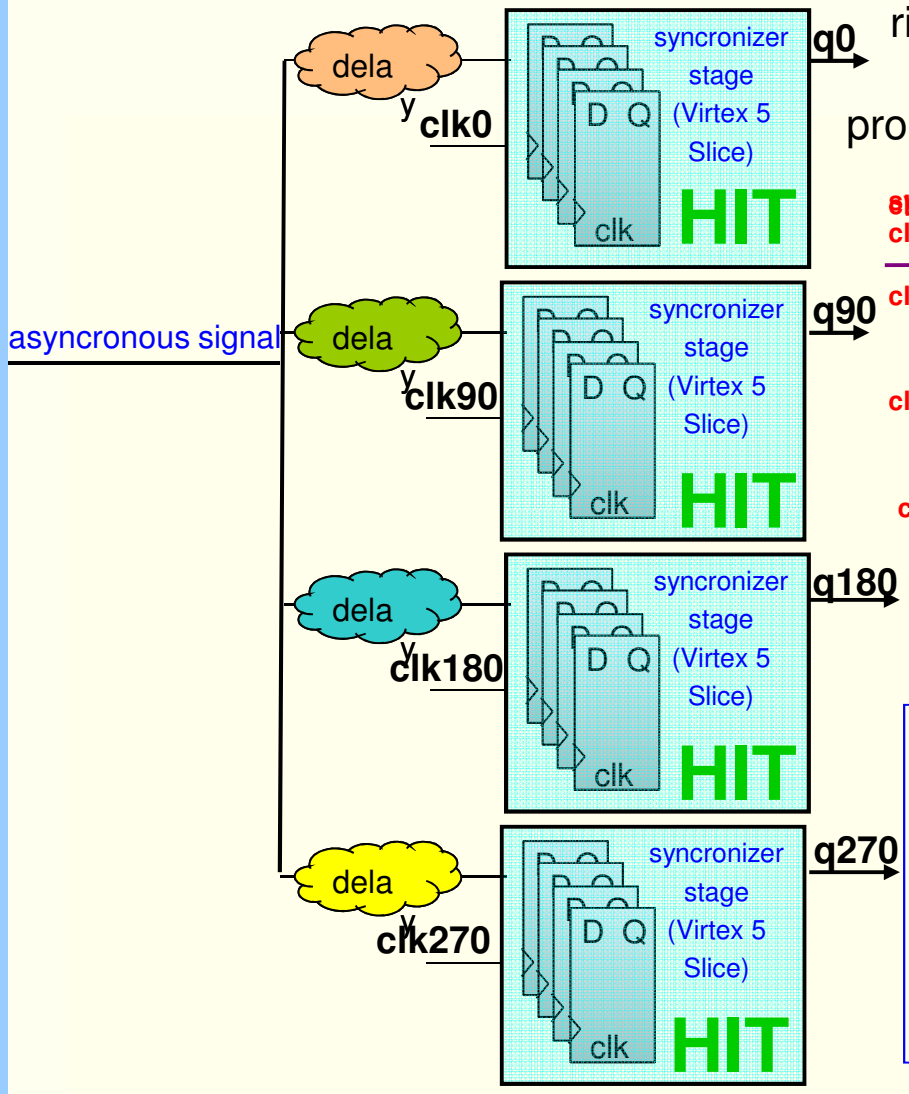
Implementation of the TDC in the Xilinx XC5VLX50 FPGA



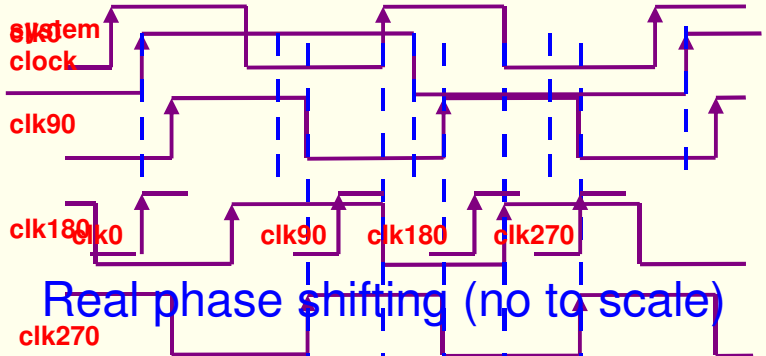
Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	2,914	28,800	10%
Number used as Flip Flops	2,914		
Number of Slice LUTs	1,055	28,800	3%
Number used as logic	1,038	28,800	3%
Number using O6 output only	499		
Number using O5 output only	30		
Number using O5 and O6	509		
Number used as exclusive route-thru	17		
Number of route-thrus	53	57,600	1%
Number using O6 output only	47		
Number using O5 output only	6		
Slice Logic Distribution			
Number of occupied Slices	888	7,200	12%



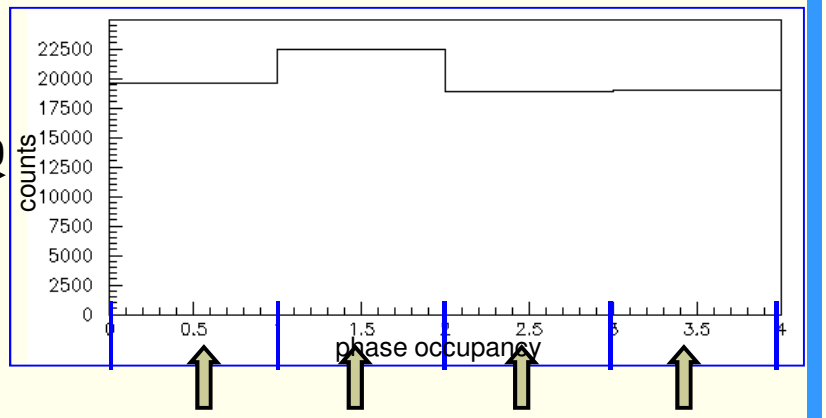
Phase detecting(2)



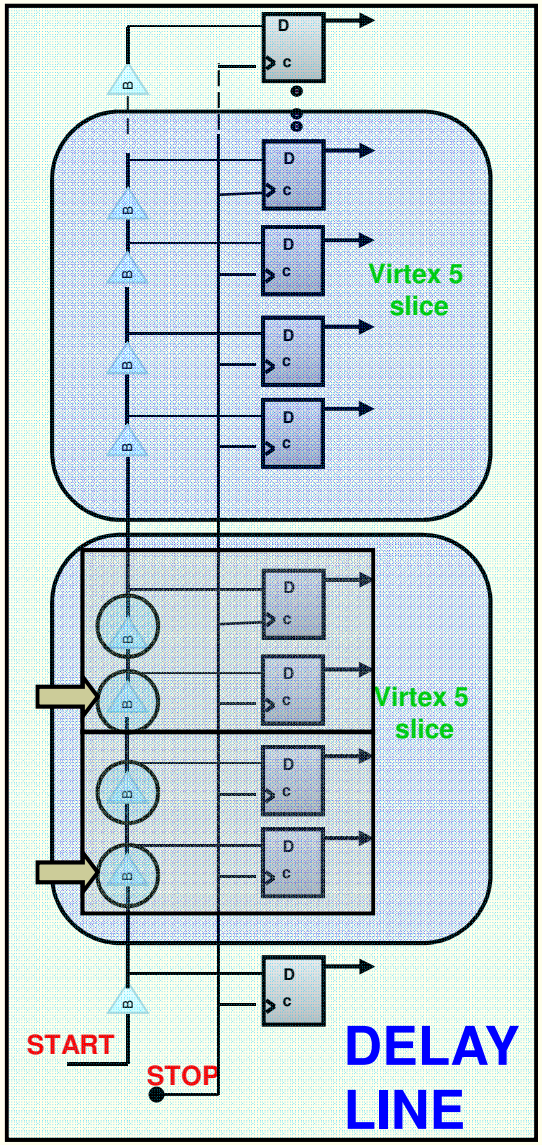
The measure of the phase occupancy of the rising edge of an asyncronous signal will depends from the skew of the signal propagating through the syncronizing stages.

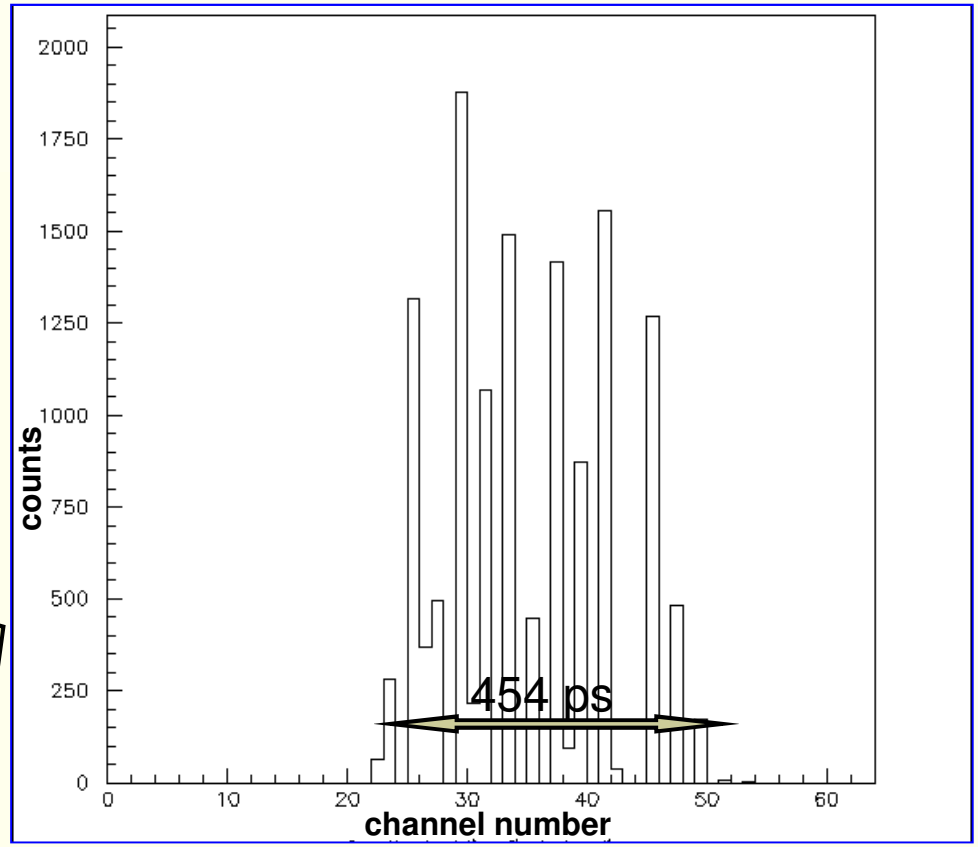


The asyncronous signals skew can be simplified as a clock signals deviation from the ideal behavior.



Delay line non linearity





The slice is divided in two substructure made of couple of flip-flop.
The propagation time of the first and the third buffer inside the slice are so low that:
the first couple of flip-flop switch always together,
while the second couple of flip-flop switch often together.
The mean propagation time of every buffer of the line is 13 ps.

High Stability Oscillators

VFTX140

Features:

- ✓ 550 MHz frequency;
- ✓ LVPECL output levels;
- ✓ 3.3 V supply voltage;
- ✓ Operating temperature range between 0℃ and 70℃ ;
- ✓ Frequency stability vs operating temperature is less than 0.28 ppm;
- ✓ Frequency stability on overall conditions (including aging 20 years) is less than 4.6 ppm.

VFOV200

Features:

- ✓ 250 MHz frequency;
- ✓ HCMOS output levels;
- ✓ 3.3 V supply voltage;
- ✓ Operating temperature range between -30℃ and 70℃ ;
- ✓ Frequency stability vs operating temperature of 10 ppb;
- ✓ Frequency stability vs supply voltage of 1 ppb;
- ✓ Frequency stability vs aging/day of 0.5 ppb, aging/year 0.1 ppm.