A flash high-precision Time-to-Digital Converter implemented in FPGA technology

P. Branchini[a], S. Loffredo[a]

[a]Dipartimento di Fisica, Università Roma Tre and I.N.F.N. Sezione di Roma Tre, Rome, Italy

loffredo@roma3.infn.it

Abstract

The construction and design process of a high-resolution time-interval measuring system implemented in a SRAM-based FPGA device is discussed. A flash architecture has been implemented. The architecture used is virtually dead time free. It consists of a high precision quartz driven coarse time counter, and a two step phase interpolator. Time intervals of 50 ps steps have been generated to characterize the TDC within the clock period (1.818 ns). The behaviour of the TDC has been tested up to a 20 μs interval in 1 μs steps. In this way we have measured a resolution on the time interval of about 50 psec on every single measurement. The results of the device in terms of resolution, differential and integral non-linearity are presented.

I. INTRODUCTION

Time to Digital Converters (TDCs) are often required in many applications in High Energy and Nuclear Physics. Furthermore, they have been widely used in many scientific equipments such as Time-Of-Flight (TOF) spectrometers and distance measurements. Different configurations of tapped delay lines are widely used to measure sub-nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs lower the development cost and offer high design flexibility. Rapid progress in FPGA electronics technology allowed achieving a time resolution values in between 50 ps and 500 ps [1], [2]. The architecture used in this device beside being dead time free is multi-hit and allows for a resolution of about 50 psec. We'll show its performance in terms of resolution, integral and differential non linearity.

II. PRINCIPLE OF OPERATIONS

Our architecture is based on the newest available Xilinx Virtex-5 FPGA [3]. We used the XC5VLX50 with -3 speed grade in order to improve the performance for high-speed design. The approach exploits the classic Nutt method [4] based on a multi-stage interpolation. The first stage is built around a coarse free-running counter used to measure long time intervals. The Virtex-5 Digital Clock Managers (DCMs) provide a wide range of clock management features and allow phase shifting. We used a DCM that gives four copies of the same clock signal shifted by 0° (clk0), 90° (clk90),

180°(clk180) and 270°(clk270). The DCM output signals synchronize a state machine that is also used to perform a first phase interpolation measurement. The coarse conversion dynamic range is limited to the counter output width. The bin size of the coarse output is limited by the clock period, the DCM is used to perform a first level phase (fine time measurement) interpolation thus giving a resolution of about 454 ps. The third stage performs the iper fine time measurement thus improving the coarse counter resolution. Since we also exploit the four phases information delivered by the DCM the delay line must only interpolate in between the four different phases i.e. over a quarter of the clock cycle. Our time converter consists of tapped delay lines.

III. THE TDC TESTER BOARD

The TDC Tester board we have built is shown in Fig.1. On this board we have installed two high stability oscillators [5]. The first oscillator (VFTX140) generates an output frequency of 550 MHz. Its temperature stability is better than 0.28 ppm over a temperature range from 0°C to +70°C. The output is configured as a differential LVPECL signal. Long term time accurancy depends on oscillator stability. To address this problem the VFOV200 oscillator has been selected. This oscillator provides an HCMOS output frequency of 250 MHz and it has a temperature stability up to 5 ppb over a temperature range from -40°C to +85°C. Test points for high-bandwidth active probes are used to perform the Virtex-5 clock signal characterization. SMA connectors are used to send the start and stop signals to the device. They may adopt differential or single-ended signalling schemes. The Tester daughter board is hosted by a VME module wich allows us to test and read-out the TDC via a VME CPU.

IV. TDC ARCHITECTURE

The simplified circuit block diagram of the TDC architecture is shown in Fig.2. The external clock frequency we used was 550 MHz. The coarse time measurement is obtained by the TDC using quartz clock signal. The task of the finite state machine shown in Fig.3 is to select the proper delay line and perform a first phase interpolation using the 4 phases of the clock and delivering a fine time measurement. A 2 bit counter N_c encodes the value of the difference of the first step phase interpolator. Delay lines have been used to interpolate the

phase within a quarter of the clk period and thus improving the time resolution and delivering an iper fine time measurement.

Fig.2, follow the phase difference between the start/stop and the clk0 signal.

This value is "00" if the phase difference is between 0 and $\pi/2$,
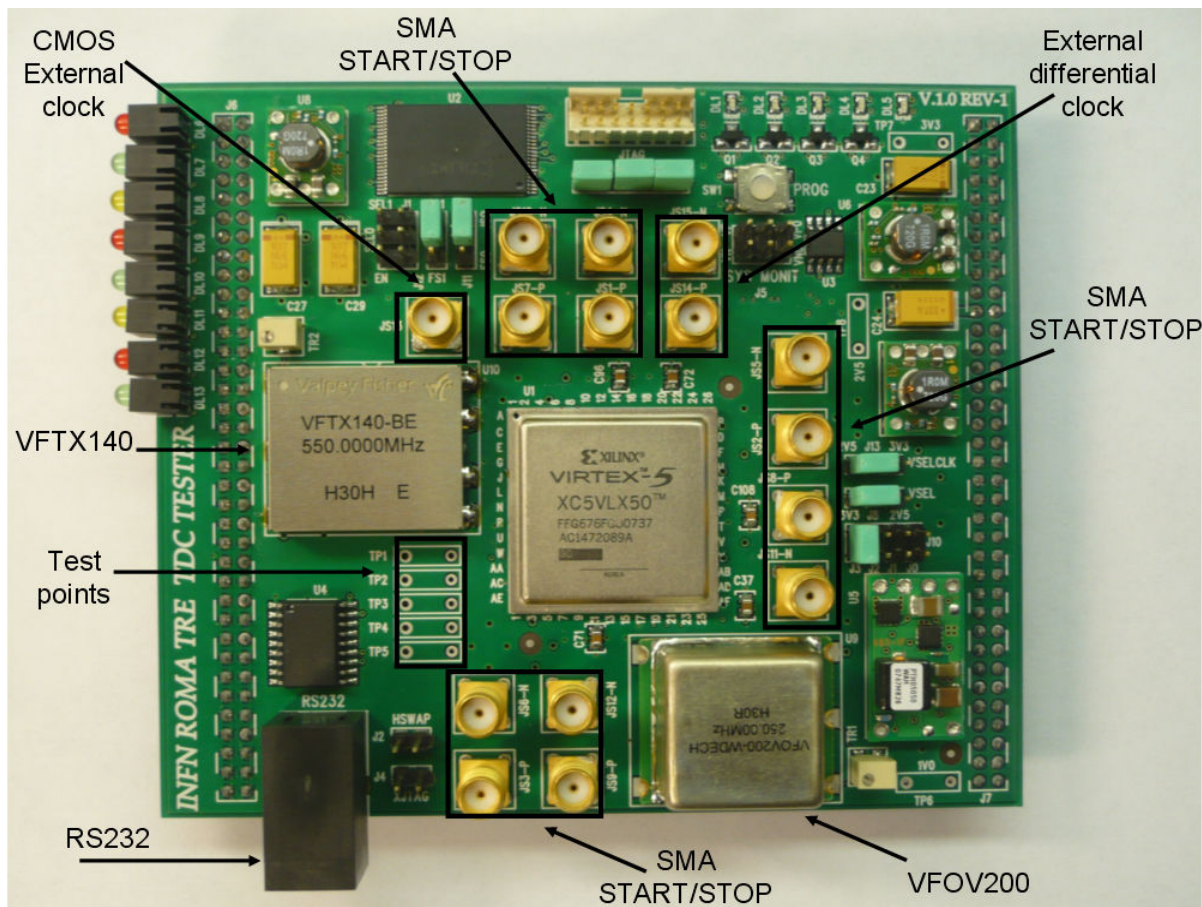

Figure 1: The TDC tester board

The building blocks of the coarse TDC are the 550 MHz synchronous binary counter and the finite state machine. The coarse counter has a 32 bit data width and is used in free-running mode. This counter is reset only at power up. When the start signal transition occurs the current state of the counter is sampled by the start register, and the same operation occurs also when the stop signal is delivered to the TDC. The difference between the stop and the start register is the coarse measurement of the time interval. The state machine samples the start and the stop signal and detects the phase difference between the start and stop rising edges. The least significant bit corresponds to a quarter of the clock period. The full clock period is recovered by the 2 bit counter $N_c[1:0]$ which labels the phase value. The output binary value $N_c[1:0]$ increases the data out width of the coarse TDC, N_c which is a 34 bit wide word. Therefore the state machine allows us to obtain a time resolution of quarter of the clk0 period (454 ps). The delay line therefore is only used to interpolate the phase in one quarter of the clock period. The sel0/1[1:0] outputs, shown in

"01" if it is between $\pi/2$ and π, "10" if it is between π and $3\pi/2$, and "11" if it is between $3\pi/2$ and 2π. The selection of the tapped delay line of the fine time measurement reflects the phase difference between the start/stop signal and clk0. The measurement range of the coarse TDC is limited due to the counter width and the resolution is limited due to the clock frequency.

V. CARRY CHAIN DELAY LINE

The carry chain delay line is shown in Fig 4. We have used high-speed chain structures that vendors designed for general-purpose applications. In this configuration the stop signal is the 550 MHz system clock. The start signal after each delay unit is sampled by the corresponding flip-flop on the rising edge of the stop signal. In this configuration the delay line consists of set of 64 multiplexers in sequence. The selection bit of every multiplexer is set to logic value one, in order to let the start signal propagate through the line. The time quantization step of the TDC is determined by the multiplexer

propagation delay time τ. Due to the short delay of the tapped delay line, it's necessary to use four delay lines in order to cover the full clock period. The four lines are clocked by the

binary natural code by using a priority encoder. A very short dead time (about 1 clock period) is the main advantage of using the carry chain delay line.
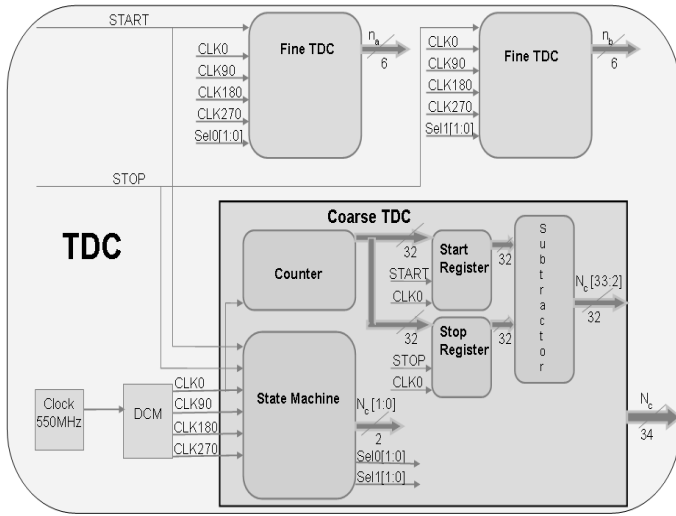

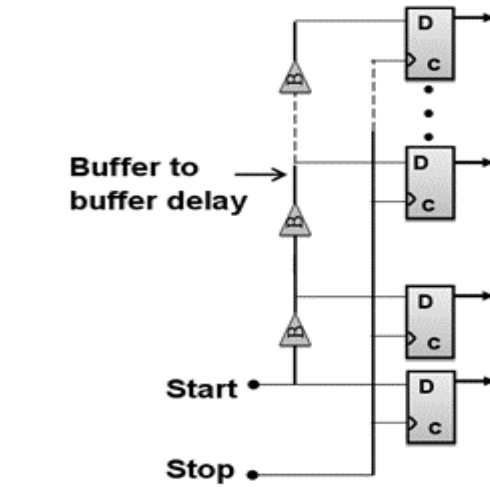Figure 2: Simplified circuit block diagram of the TDC architecture.

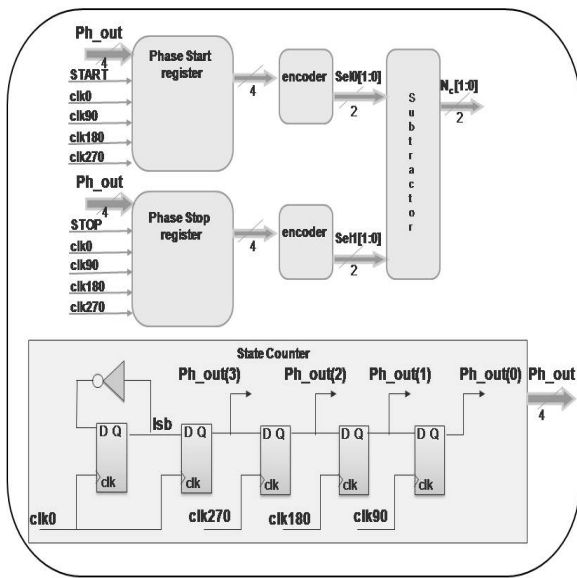Figure 4: Logic block diagram: Carry chain delay line.

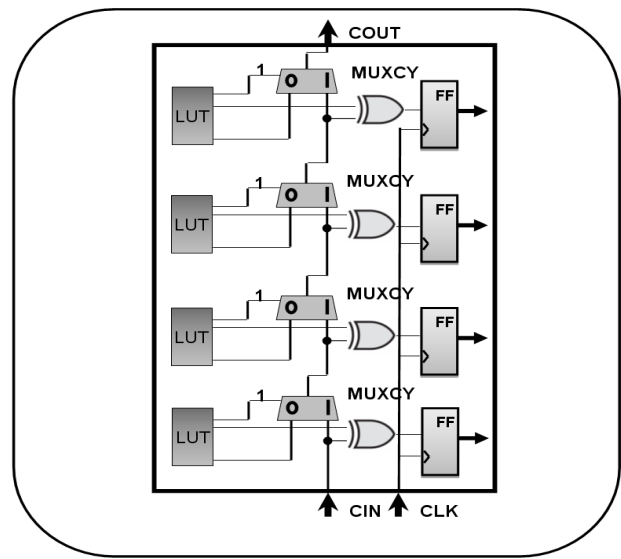Figure 3: Simplified block diagram of the finite state machine.

Figure 5: Simplified circuit block diagram of the Virtex-5 slice.

VI. TESTING THE TDC

clk0, clk90, clk180, clk270 signals delivered by the DCM. The state machine selects the right delay line by asserting the sel0/1[1:0] bits. In Fig. 5 a simplified block diagram of the Virtex-5 slice is shown. The carry chain delay lines are implemented in a small region of the device and every line uses 8 slices of it. We decided to use four delay lines rather than one but longer, in order to reduce the possible non linearity introduced by the clock distribution between neighbouring slices. Furthermore in this way, the output from the tapped line is converted from thermometric code into

To perform our tests we have used an architecture based on an off-the-shelf CPU board, the Motorola MVME6100[6]. The CPU board is designed around the MPC7457 PowerPC processor running at 1.267 GHz. The VME board hosting the TDC Tester daughter card can handle A32/D16 VME cycles and is configured as slave. We have used a DTG5334 [7] as a pulse generator. The DTG5334 can deliver time intervals as long as 20 μsec in 1 ps step. Since we have operated the DTG in free running mode an accept signal was delivered by the MVME6100 to the VME slave board in order to start and stop

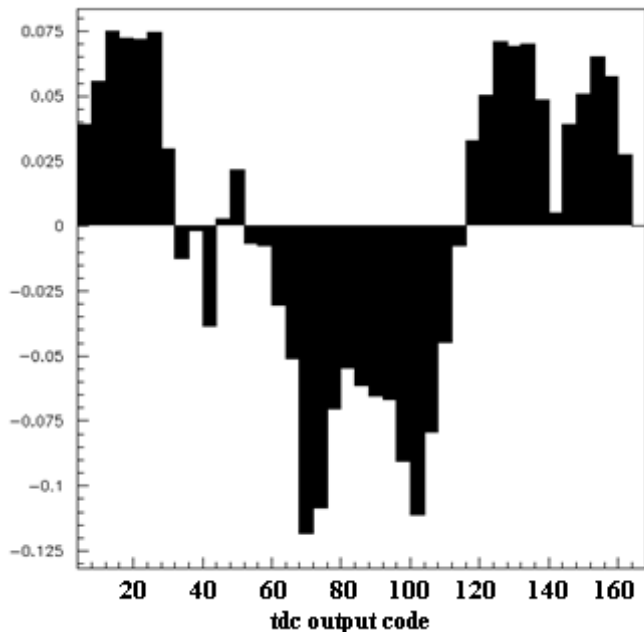measurements. The TDC is linear up to 20 µsec
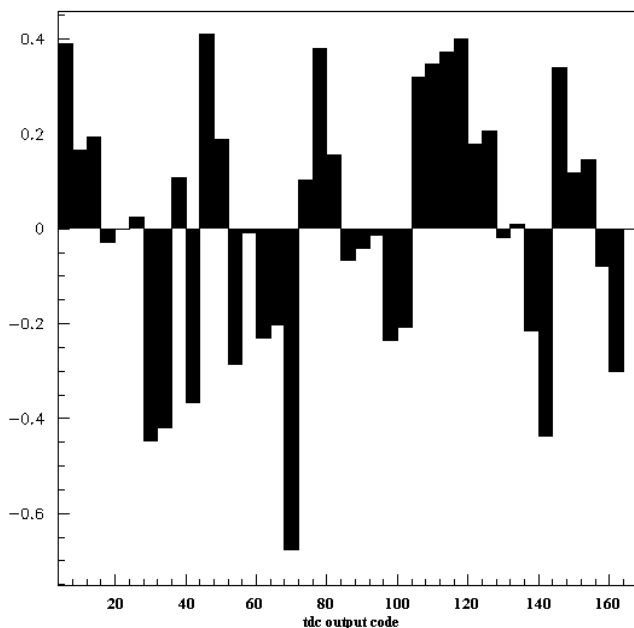

Figure 6: Integral non linearity.

Figure 7: Differential non linearity

and we have measured a resolution of about 50 psec in every measured point in that time interval.

In figure 6 we show on a 2 nsec interval the integral non linearity as a function of the TDC output code. In the same time interval figure 7 shows the differential non linearity.

VII. CONCLUSIONS

A TDC based on a FPGA architecture has been built. The advantage of the TDC delay line architecture implemented in FPGA is the ease of use and flexibility. FPGA electronics

technology allows to achieve high speed digital designs. This means high resolution digital counter and then a reduced number of delay elements of the line used for the time interpolation within the system clock cycle. The architecture implemented shows very good performance in terms of time resolution (about 50 psec up to 20 µsec) and very low dead-time.

VIII. ACKNOWLEDGMENTS

IX. REFERENCE

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