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A flash high-precision Time-to-Digital Converter implemented in FPGA technology

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Time to Digital Converters (TDCs) are often required in many applications in High Energy and Nuclear Physics. Furthermore, they have been widely used in many scientific equipments such as Time-Of-Flight (TOF) spectrometers and distance measurements. Different configurations of tapped delay lines are widely used to measure sub-nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs lower the development cost and offer high design flexibility. Rapid progress in FPGA electronics technology allowed achieving a time resolution values in between 50 ps and 500 ps .
The architecture used in this paper beside being dead time is multi-hit and allows for a
resolution of about 35 psec. We'll show in this paper its performance in terms of resolution,
integral and differential non linearity

Summary

The construction and design process of a high-resolution time-interval measuring system implemented in a SRAM-based FPGA device is discussed in this paper.
A flash architecture has been implemented. The architecture used is dead time free.
Pulses with a jiitter less than 0.5 psec between the start and stop signal have been generated over a time interval of 20 musec.
In this way we have measured a resolution on the time interval better than 35 psec on
every single measurement.
The results of the device built in terms of resolution differential and integral non-linearity are
shown in this paper.

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