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The Fast Tracker Architecture for the LHC baseline luminosity

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Hadron collider experiments search for extremely rare processes hidden in much larger background levels. Only a tiny fraction of the produced collisions can be stored on tape and an enormous real-time data reduction is needed. This requires massive computing power to minimize the online execution time of complex algorithms. A multi-level trigger is an effective solution for an otherwise impossible problem.

The Fast Tracker (FTK) [1], [2] has been proposed for high quality track finding at very high rates (Level-1 output rates) for LHC experiments. FTK will use FPGA and ASIC devices in order to complement CPUs. FTK beats the combinatorial challenge with special associative memories, where parallelism is exploited to the maximum level. They compare the track detector hits to all pre-calculated track patterns at once.

The system design is defined and proposed for high-luminosity studies including low-Pt B physics and high-Pt signatures for Level-2 selections: b-jets, tau-jets, and isolated stiff light leptons. We test FTK algorithms using Atlas full simulation with WH and Hqq events at 10⁻³⁴ cm⁻² s⁻¹. The reconstruction quality is evaluated comparing FTK results with the tracking capability of an offline tracking algorithm. We show that similar resolutions and efficiencies are reached by FTK. The online use of the whole silicon tracker is necessary to obtain the low fake rate typical of the offline. We study the event timing inside the pipelined, data-driven FTK architecture. We compare different architectures to optimize the latency and hardware system size.

FOOT Notes.

 The fast tracker processor for hadronic collider triggers, Annovi, A et al.; ;
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