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A 40 MHz trigger-free readout architecture for the LHCb experiment

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LHCb is considering an upgrade towards a full 40 MHz readout. In this paper we investigate possibilities for a new Timing and Fast Control (TFC) system based on completely new technologies, and the consequences for the readout electronics. We define the requirements and propose an architecture allowing partitioning, complete readout control and event management. The backbone is based on bidirectional high-speed optical links using the latest FPGA transceivers. For the Front-End Electronics we advocate exploiting the bidirectional capability of the CERN GigaBit Transceiver to make the Readout Boards the TFC and the Control System interface to the Front-End.

Summary

The LHCb experiment at CEN is considering an upgrade towards a trigger-free 40 MHz complete event readout to a farm performing the event selection with only a high-level software trigger with access to all detector information. This allows operating LHCb at ten times the current design luminosity and improving the trigger efficiencies in order to collect more than ten times the statistics foreseen in the first phase. In practice it requires replacing the entire readout system. Optical links based on the CERN GigaBit Transceiver (GBT) are considered for the readout between the front-end electronics (FE) and a set of 400 Readout Boards. The Readout Boards will act as interfaces to the event-building 16 Terabit/s readout network based on IP-Over-InfiniBand. Exploiting the bidirectional capability of the CERN GBT, the Readout Boards also act as the FE interface for timing and synchronous control information, as well as the bridge for configuration and monitoring information on a subset of the optical links. The event filter farm is to be based on COTS multicore computers.

In this paper we present the architecture in consideration. In particular, we investigate new technologies and protocols to build a system for the distribution of timing, and synchronous and fast asynchronous control commands. This so called Timing and Fast Control (TFC) system sequences resets and calibrations, produces auto-triggers and performs rate control and central destination control for the events. It also manages the load balancing of the readout network and the event filter farm. The TFC system will be centred on a single FPGA-based multimaster allowing parallel stand-alone operation of any subset of sub-detectors. The TFC distribution network between the TFC master and the Readout Boards under investigation consists of a bidirectional optical network based on the high-speed transceivers embedded in the latest generation of FPGAs (ALTERA Stratix IV) with special measures to have full control of the phase of the transmitted clock and the latency of the transmitted information. Since data zero-suppression is performed at the detector front-ends, the readout is effectively asynchronous and will require that the synchronous control information carry event identifiers to allow realignment and synchronization checks.

For the detector FE we advocate exploiting the bidirectional capability of the CERN GBT development to also make the Readout Boards the relay for timing and synchronous control information, as well as the bridge for configuration and monitoring information on a subset of the optical links.

Recognizing the expanse of the LHCb upgrade, the new TFC architecture allows hybrid operation with the old and new readout electronics.

At the end we demonstrate the usefulness of a complete simulation framework and discuss the necessary R&D studies we are undertaking. We also underline the importance to take lead with the development of the TFC system in order to facilitate tests and assure conformity of the sub-detector electronics with the common specifications.

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