Calibration of the Prompt L0 Trigger of the Silicon Pixel Detector for the ALICE Experiment

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Abstract

The ALICE Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment at LHC. It includes 1200 front-end chips, with a total of ~10^7 pixel channels. The pixel size is 50 x 425 μm^2. Each front-end chip transmits a Fast-OR signal upon registration of at least one hit in its pixel matrix. The signals are extracted every 100 ns and processed by the Pixel Trigger (PIT) system, to generate trigger primitives. Results are then sent within a latency of 800 ns to the Central Trigger Processor (CTP) to be included in the first Level 0 trigger decision.

This paper describes the commissioning of the PIT, the tuning procedure of the front-end chips Fast-OR circuit, and the results of operation with cosmic muons and in tests with LHC beam.

I. System Description

ALICE (A Large Ion Collider Experiment) is one of the experiments at the Large Hadron Collider (LHC) at CERN, optimized to study the properties of strongly interacting matter and the quark-gluon plasma in heavy ion collisions [1][2].

The ALICE experiment is designed to identify and track particles with high precision over a wide transverse momentum range (100 MeV/c to 100 GeV/c). ALICE will also take data with proton beams, in order to collect reference data for heavy ion collisions and to address specific strong-interaction topics for which ALICE is complementary to the other LHC detectors.

The Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment, providing vertexing and tracking capabilities [5][6][7]. As shown in Figure 1, the SPD is a barrel detector with two layers at radii of 3.9 cm and 7.6 cm, respectively, from the beam axis. The minimum distance between the beam pipe and the inner layer is ~5 mm. The SPD consists of 120 detector modules, called half-staves. Each of them includes two silicon pixel sensors, flip chip bump bonded to 10 front-end readout chips realized in a commercial 0.25 μm CMOS process. One front-end chip contains 8192 pixel cells organized in 32 columns and 256 rows. The pixel dimensions are 425 × 50 μm^2 (z × rφ); in total there are 9.83 × 10^6 pixels in the SPD. In order to maintain the material budget constraint of 1% X_0 per layer, the sensor chosen thickness is 200 μm and the pixel chips are thinned to 150 μm. Signal and power connections for the chips are provided by an aluminium multilayer bus, glued on top of the ladders.

The 10 front-end chips of each half-stave are connected to a Multi Chip Module (MCM). The MCM contains 4 ASICs and one optical transceiver module: they provide timing, control and trigger signals to the chips. The MCM performs the readout of the front-end chips sending the data to the off-detector electronics in the control room [8]. The MCM is connected to 3 single mode optical fibers; two of them are used to receive the serial control and the LHC clock at 40.08 MHz, and the third is used to send the data to the off-detector electronics.

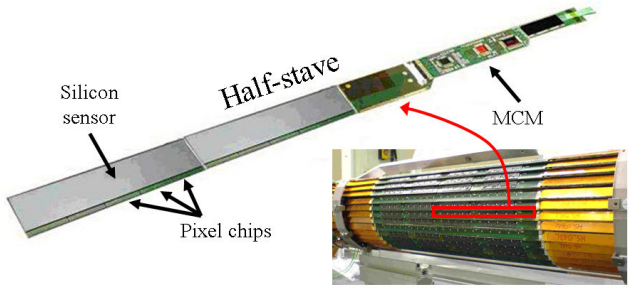

Figure 1: SPD (right) and one half-stave (left)

Each of the 1200 front-end chips of the SPD may activate its Fast-OR output every 100 ns when at least one pixel inside the chip is hit by a particle. The 1200 Fast-OR bits are sampled and transmitted to the off detector electronics by the MCM. The Fast-OR generation capability is a unique feature among the vertex detectors of the LHC experiments. It allows the SPD to act also as a low latency pad detector that can be added to the first level trigger decision of the ALICE experiment.

The Pixel Trigger (PIT) system [9] was designed to process the Fast-OR bits and produce a trigger output for the Level 0 trigger decision. It is composed of 10 OPTIN boards that receive the data streams coming from the 120 modules of the SPD and extract the Fast-OR bits; the OPTIN boards are mounted on a 9U board, called BRAIN, with a large FPGA (called Processing FPGA, type Xilinx Virtex4) that can apply

up to 10 algorithms in parallel on the 1200 Fast-OR bits every 100 ns.

The algorithms are based on topology and multiplicity, and they are implemented using boolean functions.

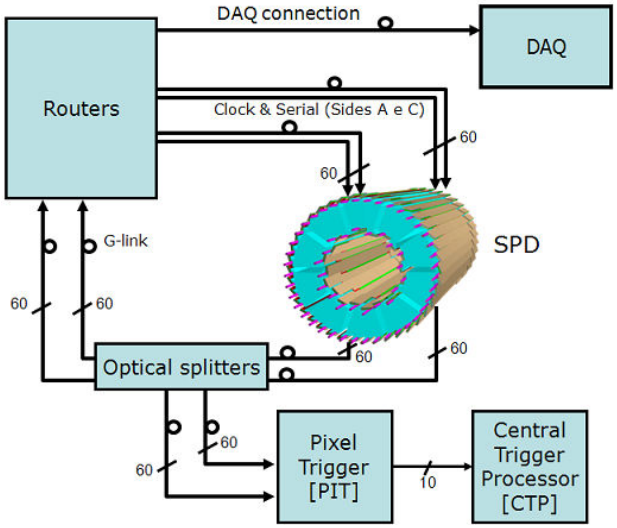

Figure 2: Pixel Trigger integration

The system integration is shown in Figure 2: the 120 optical fibers for the SPD data (60 per SPD side) are connected to 120 optical splitters, located in the rack next to the CTP. One output of the splitters goes to the routers, located in the control room, for the readout operations, the other output goes to the Pixel Trigger system. The outputs of the Pixel Trigger are sent to CTP of ALICE within 800 ns from the particle collision, to comply with the experimental requirements.

The SPD and the Pixel Trigger control systems are two independent systems; both of them have software drivers implemented in C++ in the Front End Device (FEDs) servers. There are in total two driver systems (spdFed) for the SPD, one per side of the detector, and one driver system (pitFed) for the Pixel Trigger. All the FED systems (spdFed and pitFed) have User Interfaces accessible by an operator through the PVSS II supervision layer [11].

II. Fast-OR tuning

Every chip contains 42 internal DACs, 8 bits each, to provide voltage and current biases to the analog and digital circuitry of the chip. In every chip there is a dedicated Fast-OR circuitry controlled by four DACs. The DAC settings affect the efficiency, uniformity and noise immunity performances of the Fast-OR circuitry.

Table 1: Fast-OR DACs

DAC name	
Fast_FOPOL	Fast-OR current pulse source
Fast_CONVPOL	Current mirror voltage bias
Fast_COMPREF	Comparator reference at the end of the Fast-OR chain
Fast_CGPOL	Transconductance fine tuning

Tuning of all the SPD modules is required in order to maximize the sensitivity of the detector to single hits and minimize the readout noise of the Fast-OR trigger signal. This has to be done individually for each of the 1200 front-end chips of the SPD.

An initial manual procedure for the tuning has been carried out in the laboratory, in order to study the behaviour of the circuitry responsible of the triggering and to model the impact of the DAC settings on the Fast-OR signal.

The tuning procedure makes use of the possibility to apply a test pulse in every pixel. The test pulse was sent to some pixels inside the chip to simulate the charge generated by a Minimum Ionizing Particle (MIP) going through the sensor. The tuning of the Fast-OR is based on a comparison between the number of test pulses sent to a chip, and the number of Fast-OR pulses detected at the input of the Pixel Trigger for this particular chip. The Fast-OR pulses are counted by counters implemented in each OPTIN board.

The laboratory tests have shown that changing the DAC values can highly affect the Fast-OR signal behaviour. It has been verified the existence of an optimum range of settings for which the efficiency of the Fast-OR signal is high (>95%). With different DAC settings the chip can become totally inefficient or noisy.

III. Automatic tuning procedure

The automatic procedure for the Fast-OR tuning was then developed in order to

1. reduce the time needed to calibrate all the DACs of all the 1200 front-end chips of the SPD;
2. determine values and ranges for all the readout chips with guaranteed efficiency, timing and uniformity performances.

On the basis of the experience gained with the manual calibration, some criteria are applied to optimize the automatic tuning procedure, to reduce the complexity and the time needed for the calibration.

The number of DACs to scan for optimum settings can be limited to four: one DAC that corresponds to the general threshold of the chip and 3 Fast-OR DACs. Table 2 indicates the DACs included in the automatic procedure and their effect on the Fast-OR signal.

Table 2: DACs included in the tuning procedure

DAC name	Effect on Fast-OR
Pre_VTH	global threshold of the chip
Fast_FOPOL	efficiency and uniformity
Fast_CONVPOL	efficiency and uniformity
Fast_COMPREF	digital noise immunity

These DACs are scanned over a programmable range set by the operator: the scan can be limited to the optimum range found with the manual tuning. For every DAC setting, the Fast-OR counts in the Pixel Trigger are compared to the number of test pulses sent to the chips.

The Fast-OR efficiency is verified in different operating conditions:

- when none of the pixels is activated by a test pulse (to check the noise of the Fast-OR signal during the readout);
- when only one pixel is activated by a test pulse;
- when more than one pixel is activated, without exceeding the maximum occupancy of the chip (~12%).

The Fast-OR tuning procedure can be done in parallel for all the 1200 chips of the SPD.

A. Implementation

The components involved in the Fast-OR automatic tuning procedure are presented in Figure 3.

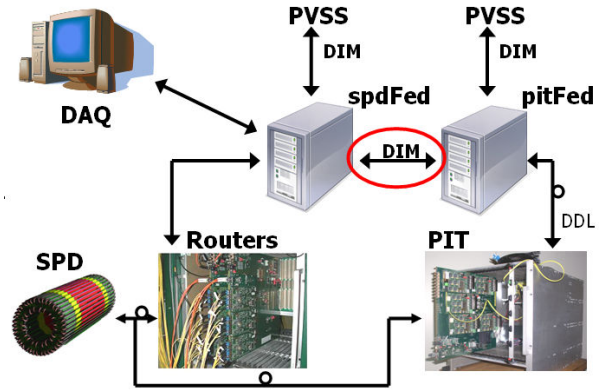

Figure 3: Components involved in the calibration

The Fast-OR tuning is managed by the driver system of the SPD, similarly to several other calibration scans. A C++ class has been implemented and the flow diagram of the main operations performed is shown in Figure 4.

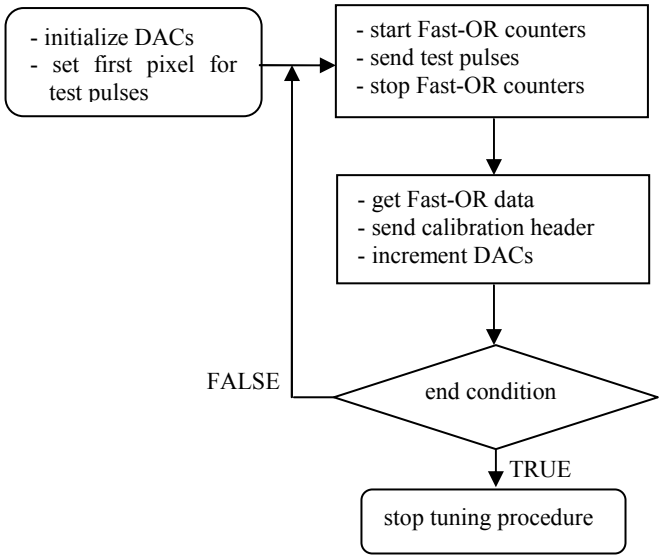

Figure 4: Structure of the Fast-OR calibration class

The spdFed servers interact with the SPD to loop over the DAC values and to define the pixel to receive the test pulses. They also communicate with the Pixel Trigger to retrieve the Fast-OR data, using commands already implemented in the Pixel Trigger driver.

A new communication layer has been established between the SPD and the Pixel Trigger driver systems. It is based on the Distributed Information Management (DIM) system developed at CERN. The Fast-OR counters of the Pixel Trigger corresponding to the two SPD sides are managed separately, to avoid interferences during the scan.

Once the information of the Fast-OR counters is retrieved by the spdFed, a calibration header is built and then sent to the acquisition system. A Detector Algorithm, based on custom developed C++ classes within the ALICE offline framework, analyzes the data contained in the header and finds for each SPD chip a good DAC combination [12].

The Detector Algorithm analyzes every DAC combination; the DAC values that can satisfy the efficiency requirements for all the pixel configurations activated in a chip are selected. The final DAC settings to be applied are decided finding per each DAC the most frequent value among the ones that have overcome the first selection.

The efficiency requirements during the data analysis can be set with tolerances of up to 5%.

B. Results of the procedure

Figure 5 shows a typical result of the Fast-OR calibration: the procedure has been applied over the full range of the DACs, the Fast-OR is plotted as a function of the two DACs Fast_CONVPOL and Fast_FOPOL. Three different regions can be identified:

- inefficiency, dark area with Fast-OR counts near zero;
- noise, bright area with very high Fast-OR counts;
- good region, area with Fast-OR counts equal to the number of test pulses sent.

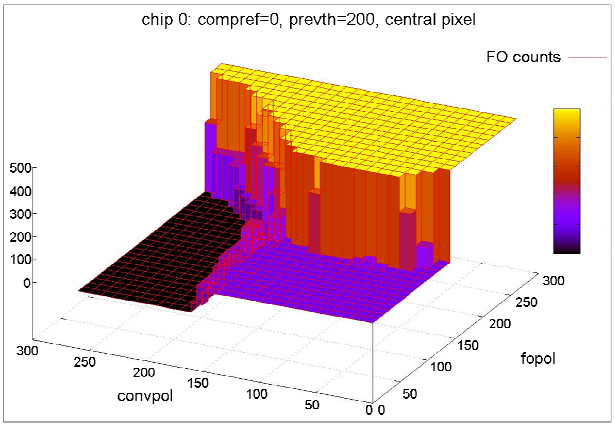

Figure 5: Fast-OR plotted as a function of two Fast-OR DACs

Since the beginning of the commissioning, the Fast-OR tuning have been applied on 105 half-staves, and in these tested half-staves the 1006 chips have been successfully calibrated. The remaining chips are masked in the trigger logic because of noise problems.

For the majority of chips (>95%) it is possible to find DAC values that have a 100% efficiency: the Fast-OR counts

at the input of the Pixel Trigger are exactly the same number as the test pulses sent to the pixels.

Table 3 resumes the status of the calibrated modules of the SPD. The percentage of the operating chips is calculated with respect to the number of tested half-staves.

Table 3: Status of the Fast-OR calibration

Tested half-staves	Inner layer	33 / 40 (82.5%)
	Outer layer	72 / 80 (90.0%)
	TOTAL	105 / 120 (87.5%)

Operating chips	Inner layer	315 / 330 (95.5%)
	Outer layer	691 / 720 (96.0%)
	TOTAL	1006 / 1050 (95.8%)

The time needed for the tuning procedure depends on the number of half-staves included in the scan and on the ranges applied to the DACs. With DAC ranges that minimize the scan over the inefficient and noise area in the parameter space (see Figure 5), a tuning of the entire detector can be done in less than 4 hours. This is two orders of magnitude less than the time needed for the manual tuning.

IV. Operation of the Pixel Trigger System

The Pixel Trigger system could be successfully used as a trigger during the commissioning phase of the SPD and of the other detectors in ALICE since May 2008. This was possible only after the tuning of the Fast-OR circuitry of all the front-end chips.

The first operation of the Pixel Trigger system was during the acquisition of cosmic rays, with a topology based algorithm of top-outer-bottom-outer layer coincidence: the output of the Pixel Trigger is active when a particle activate at the same time at least two chips, one in the upper part of the SPD outer layer, and the other in the lower part of the outer layer. Figure 6 shows a cosmic event with one muon track in the SPD online display.

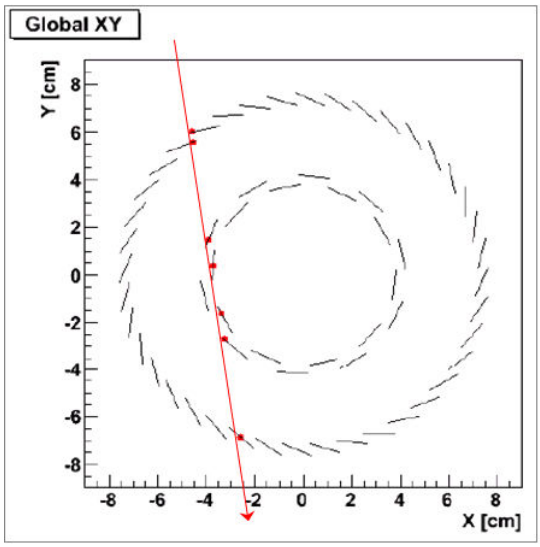

Figure 6: Cosmic ray in the SPD online display

The flux of cosmic muons in the ALICE cavern has been measured: the rate of a single muon is 3-4 Hz/m^2, resulting in an average rate through the SPD of ~1.5 Hz. The trigger rate at the output of the Pixel Trigger system ranges from 0.09 to 0.18 Hz depending on the number of active half-staves; this confirms the efficiency of the Fast-OR tuning.

During the two periods of cosmic runs in ALICE (May – Oct 2008 and Jul – Aug 2009) nearly 110k tracks were acquired with at least 3 clusters in the detector, with the trigger provided by the Pixel Trigger. These tracks show a high purity of more than 99.6%. The runs with cosmics are very useful to study the alignment of the detector modules, and of the SPD with respect to the other detectors of the Inner Tracking System.

The Pixel Trigger system and the SPD were also operated during injection tests toward ALICE: the beam was dumped before the ALICE cavern and the muons resulting from the dump went through the ALICE detectors. Events with high occupancy were recorded using a multiplicity algorithm. Figure 7 shows an example of a recorded event during the injection test of July 2009. It is possible to see long tracks crossing the 200 μm thick silicon sensors.

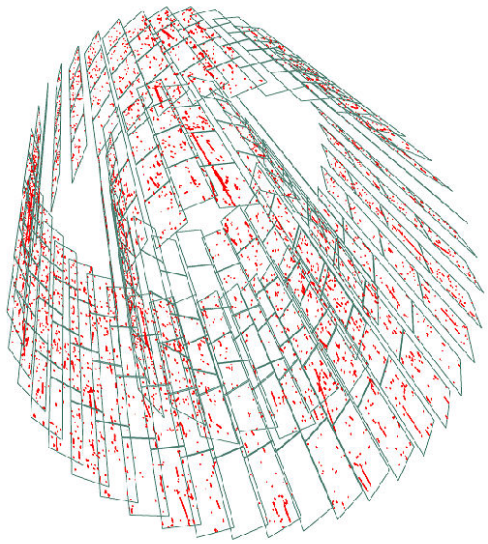

Figure 7: Event display of a particle shower during injection tests (July 2009). The two layers of the SPD are shown.

Beam-induced interactions were also observed in the ALICE Inner Tracking System during September 2008 when the first beams were circulating in the LHC.

V. Conclusions

The ALICE Silicon Pixel Detector can generate a Fast-OR output that contributes to the first level of trigger (Level 0) of the experiment. The Pixel Trigger System was designed and implemented to process the Fast-OR signal, and since May 2008 is operating in the cosmic acquisitions and with the first beams.

A fine tuning of the Fast-OR circuitry of all the 1200 front-end chips of the SPD is required to maximize the single hit detection and minimize the noise in the trigger signal.

After studies in the laboratory, an automatic tuning procedure for the Fast-OR signal has been designed, tested and qualified in the ALICE experiment. New code was implemented in the SPD driver system to manage the calibration. The Pixel Trigger and the SPD driver systems can interact through a new communication channel. A Detector Algorithm has been specifically designed to analyze the results of the Fast-OR tuning.

A calibration scan over the full SPD can be done in less than 4 hours, with enough statistics to determine the optimum settings of the Fast-OR DACs. The percentage of operating chips is ~96%.

After the Fast-OR tuning, the SPD is successfully contributing to the Level 0 trigger of the ALICE experiment, being the only vertex detector among the other LHC experiments to be included in the trigger decision.

VI. REFERENCES

[1] ALICE collaboration,, "The ALICE experiment at the CERN LHC", *JINST 3 S08002*, 2008

[2] ALICE collaboration, "ALICE: Physics Performance Report, Volume 1", 2004, *J. Phys. G: Nucl. Part. Phys*., 30, 1517-1763

[3] ALICE collaboration, "ALICE: Physics Performance Report, Volume 2", 2006, *J. Phys. G: Nucl. Part. Phys*., 32, 1295-2040

[4] ALICE collaboration, "ALICE Inner Tracking System (ITS): Technical Design Report", Oct. 2001, *CERN-LHCC-99-012*

[5] A. Kluge et al., "The ALICE Silicon Pixel Detector (SPD)", *Nucl. Instr. and Meth. Section A*, Vol. 582, Issue 3, Dec 2007, pp. 728-732

[6] P. Riedler et al., "Production and Integration of the ALICE Silicon Pixel Detector", *Nucl. Instr. and Meth. Section A*, Vol. 572, Issue 1, 2007, pp. 128-131

[7] V. Manzari et al., "Assembly, construction and testing of the ALICE silicon pixel detector", *Nucl. Instr. and Meth. Section A*, Vol. 570, Issue 2, 2007, pp. 241-247

[8] A. Kluge et al., "ALICE Silicon Pixel on detector Pilot System OPS2003 – The missing manual", ALICE Internal notes, *ALICE-INT-2004-030*

[9] G. Aglieri Rinella et al., "The Level 0 Pixel Trigger system for the ALICE experiment", *JINST 2 P01007*, 2007

[10] G. Aglieri Rinella et al., "The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector: implementation, testing and commissioning", *Proceedings of TWEPP 2008*, Naxos, Greece, Sep. 2008, pp. 123-128

[11] C. Torcato de Matos et al., "The ALICE Level 0 Pixel Trigger driver layer", *Proceedings of TWEPP 2008*, Naxos, Greece, Sep. 2008, pp. 516-521

[12] A. Mastroserio, "Operation of the ALICE Silicon Pixel Detector with cosmics and first beams", *Proceedings of 11th ICATPP Conference*, Como, Italy, Oct. 2009