The Prompt L0 Trigger of the Silicon Pixel Detector for the ALICE Experiment

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The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost layers of the ALICE experiment apparatus. It consists of 1200 pixel chips with a total of ~9.8x10^6 channels with a pixel size of 50x425 μm^2. Each pixel chip transmits a Fast-Or signal upon registration of at least one pixel hit. These signals are extracted every 100 ns and processed by the Pixel Trigger (PIT) system. The output signal of the Pixel Trigger is then sent within a latency of 800 ns to the Central Trigger Processor to contribute to the Level 0 trigger decision. This paper describes the commissioning of the PIT, the tuning procedure of the SPD modules to obtain a good efficiency of the Fast-Or signal, and results of operation in cosmic and beam runs.

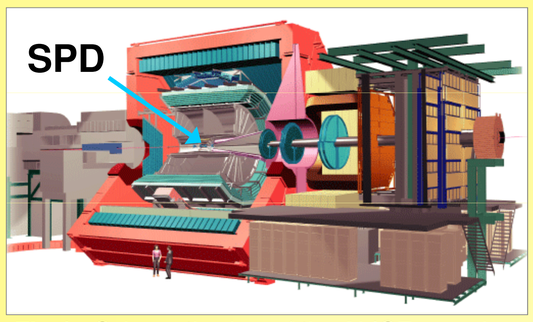

Fig.1 - Schematic view of the ALICE experiment

ALICE EXPERIMENT

- study strongly interacting matter in heavy ion collisions
- study of p-p collisions as reference data and unique physics complementary to other LHC experiments
- 0.5 T magnetic field

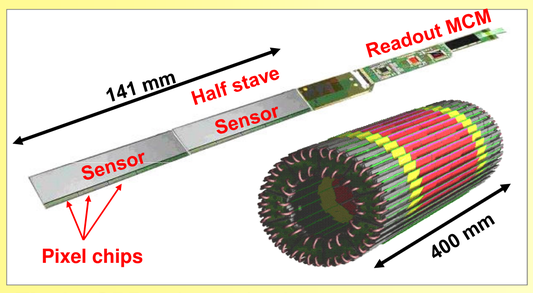

Fig.2 - SPD schematic view

SILICON PIXEL DETECTOR

- 2 barrel layers at radii of 3.9 cm and 7.6 cm
- 120 half-staves, each consisting of
  - 2 silicon sensors (70.7 x 16.8 mm^2, 200 μm thick)
  - 10 pixel chips (8192 cells, 150 μm thick)
  - 1 Multi Chip Module
  - 1 Al-Kapton multilayer flexible cable (bus)
- ~1% X_0 per layer
- ~9.8x10^6 readout channels
- pixels size 425 x 50 μm^2 (z x rφ)
- 12 μm point resolution in the bending plane

FAST-OR SIGNAL

- active on registration of at least 1 hit per pixel chip
- 1200 Fast-Or bits every 100 ns transmitted on the optical data link to the readout electronics

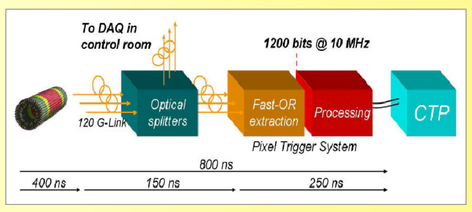

Fig.3 - Pixel Trigger hardware architecture

PIXEL TRIGGER SYSTEM

- unique feature among the vertex detectors of the LHC experiments
- dedicated system to process Fast-Or bits prior to sending to Central Trigger Processor
- contributes to ALICE L0 trigger (low latency, max 800 ns)
- **OPTIN BOARD**
  - extracts 1200 Fast-Or bits from the data stream
- **BRAIN BOARD**
  - equipped with 10 OPTIN mezzanine boards
  - processes the bits with up to 10 different algorithms at the same time

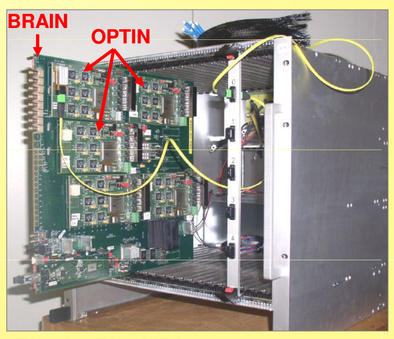

Fig.4 - Pixel Trigger crate

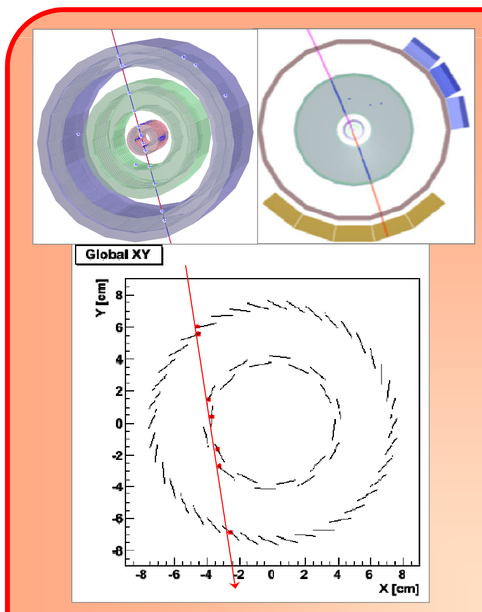

Fig.5 - Cosmic rays passing through the SPD online display (bottom) and reconstructions (top)

DATA FROM COSMIC RAYS

- coincidence between top outer layer and bottom outer layer to detect cosmic muons through SPD
- May – Oct 2008 collected ~100k tracks with at least 3 points
  - 45000 tracks with 3 clusters
  - 35000 tracks with 4 clusters
- Jul – Aug 2009 collected ~9k tracks with at least 3 points
- Pixel Trigger used also as trigger for other detectors (e.g. SDD, SSD, TPC)

DATA FROM BEAM

Trigger signal provided by the SPD

- first "sign of life" from LHC observed during the injection test in June 2008
- first beam-induced interaction observed in the ALICE Inner Tracking System (Pixel Trigger algorithm based on multiplicity) in Sep. 2008

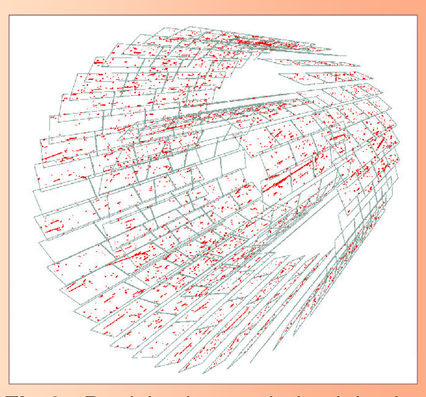

Fig.6 - Particle shower during injection test (15 June 2008)

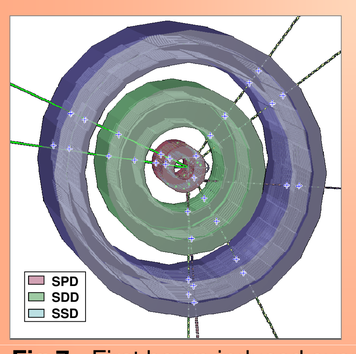

Fig.7 - First beam-induced event observed (11 Sep 2008)

FAST-OR COMMISSIONING

- baseline rate per chip: 1.4 hits/minute -> 0.023 Hz
- same rate during readout cycle -> no noise induced
- cosmics rate:
  - coincidence top - bottom outer layer: 0.08 – 0.20 Hz in agreement with Monte Carlo simulations and measured flux in the cavern
  - global OR rate: ~20 Hz

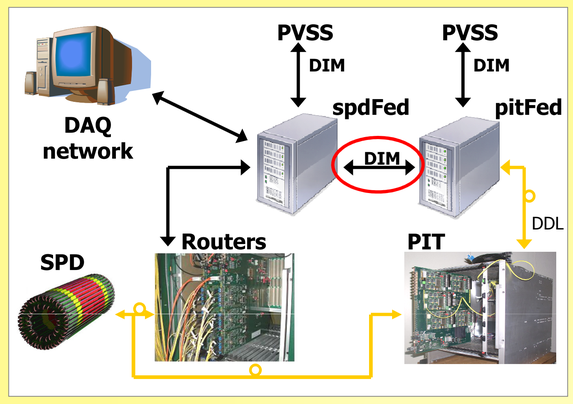

Fig.8 - Pixel Trigger integration

FAST-OR CALIBRATION

Required for every of the 1200 pixel chips to

- maximize efficiency
- minimize noise

AUTOMATIC PROCEDURE

- verify Fast-Or efficiency in different operating conditions
- compare
  - number of manual test pulses sent to SPD
  - Fast-Or counts read from Pixel Trigger
- tune a set of 4 pixel DACs per chip

COMPONENTS OF THE CALIBRATION

- SPD system
  C++ class in the Front End Device (FED) server
  ~ 600 lines of code
  – loop over DAC values
  – define pixels to activate for test pulses
  – manage communication with Pixel Trigger Fed
- Pixel Trigger system
  use of existing commands to start and stop Fast-Or counters
- Distributed Information Management
  communication layer between SPD and Pixel Trigger
  – 2 DIM services to retrieve Fast-Or data, one per SPD side to avoid interferences
  – 1 command to start and stop Fast-Or counters with separated status monitoring
- DAQ system
  – Detector Algorithm to find a good DAC combination for each chip
  – Reference Data Displayer updated to visualize the results of the calibration
- PVSS
  panel in the SPD User Interface
  – apply intervals and steps for the DACs to be tuned
  – choose pixel in the matrix to be checked

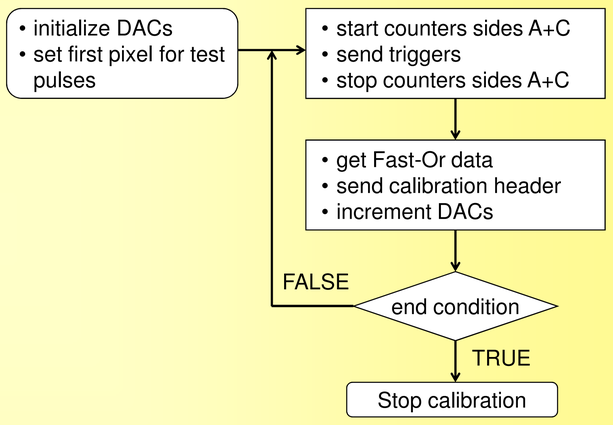

Fig.9 – structure of the C++ calibration class

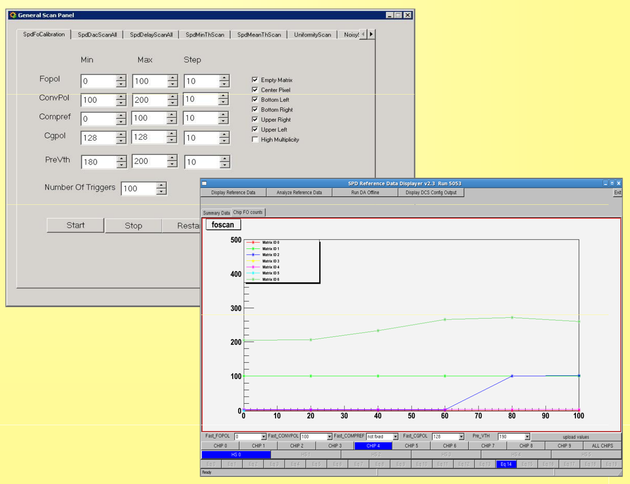

Fig.10 – PVSS panel and Reference Data Displayer

RESULTS

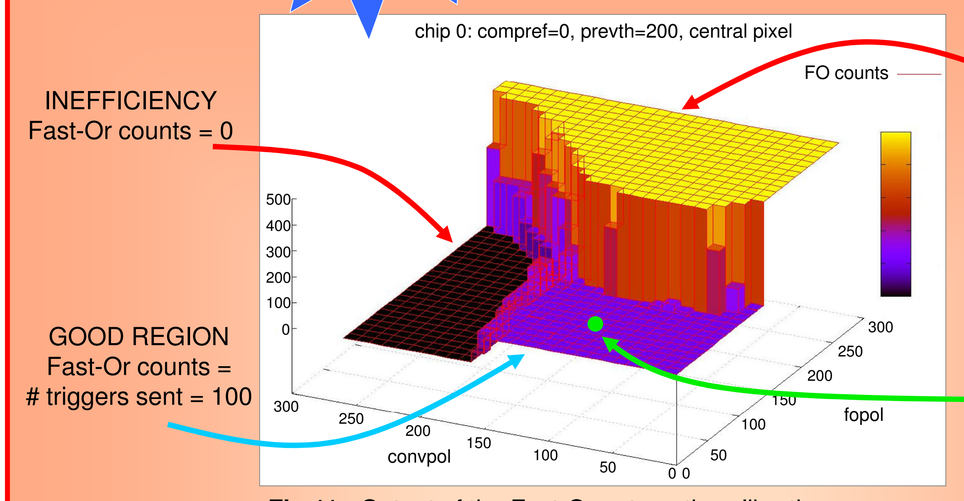

Fig.11 - Output of the Fast-Or automatic calibration (prevth, compref, convpol, fopol are the 4 Fast-Or DACs)

CALIBRATION SCANS

- Efficiency condition 100%: Fast-Or counts = # triggers sent
- Manual procedure: ~600 man-hours
- Automatic procedure: 2 to 4 hours depending on scan conditions

- Run 76245 – 83 half-staves, 20 routers
  15972 steps in 8737 seconds - data taking @ 185 Hz
- Run 77381 – 19 half-staves, 10 routers
  15972 steps in 3550 seconds - data taking @ 454 Hz

4 DACs changed
4 sets of active pixels
100 triggers per step

CALIBRATION STATUS

Tested half-staves	Inner layer	33 / 40 (82.5%)
	Outer layer	72 / 80 (90.0%)
	TOTAL	**105 / 120 (87.5%)**
Operating chips	Inner layer	315 / 330 (95.5%)
	Outer layer	691 / 720 (96.0%)
	TOTAL	**1006 / 1050 (95.8%)**

Fig.12 – Status of the calibrated chips

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on behalf of the SPD project in the ALICE collaboration