Contribution ID: **103** Type: **Poster**

The Prompt Trigger of the Silicon Pixel Detector for the ALICE Experiment

Thursday 24 September 2009 16:55 (20 minutes)

The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost layers of the ALICE experiment. It consists of 1200 pixel chips with a total of ˜107 channels with a pixel size of 50x425 μm2.
Each pixel chip transmits a Fast-Or signal upon registration of at least one pixel hit. These signals are extracted every 100 ns and processed by the Pixel Trigger (PIT) system. A signal is then sent within a latency of 800 ns to the Central Trigger Processor for the Level 0 trigger decision.
This paper describes the commissioning of the PIT, the tuning procedure of the SPD modules to obtain a good efficiency of the Fast-Or signal, and results of operations in cosmic and beam runs.

Summary

The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost layers of the ALICE experiment. It consists of 1200 pixel chips with a total of ˜107 channels with a pixel size of 50x425 μm2.
Its output data stream includes 1200 Fast-Or signals provided by the pixel chips and generated by the on-chip Fast-Or circuitry. The Fast-Or signals are transmitted every 100 ns on 120 optical links and indicate the presence of at least one pixel hit in the matrix of each readout chip. The Pixel Trigger (PIT) system extracts these signals and processes them with up to 10 trigger algorithms in parallel. Algorithms based on event topology or hit multiplicity can be implemented as boolean logic functions inside FPGAs.
The PIT sends the processed signals to the Central Trigger Processor (CTP) where they contribute to the first level trigger decision (Level 0). The PIT trigger information will help to improve event selection in proton and heavy ions collisions as well as the background rejection.
According to the design requirements, the maximum latency of the PIT output signal from the particle collision to the transmission to the CTP has been proven to be within 800 ns.
This contribution describes the commissioning of the Pixel Trigger and the tuning of the 120 SPD modules (half-staves) in order to maximize the efficiency and minimize the readout noise of the Fast-Or trigger signal. A procedure to find the optimum settings of the 4 Fast-Or internal 8-bits DACs of each pixel chip has been developed and tested in laboratory, and implemented into the experiment when the Pixel Trigger was installed in the cavern in April 2008. After an initial manual tuning, an automatic calibration procedure has been developed, with the goal to reduce by two orders of magnitude the time needed for the tuning of the 1200 pixel chips. To implement this automatic procedure, the SPD and Pixel Trigger Front End Device (FED) servers communicate to each other and exchange data through a Distributed Information Management (DIM) System. A DAC scan algorithm has been implemented inside the SPD FED Server and offline tools have been prepared to analyse the results.
The Pixel Trigger signal was successfully used by the ALICE experiment as a L0 trigger. A sizeable amount of cosmic data for alignment has been collected with several ALICE detectors being triggered by the SPD. In 6 months of operation nearly 100k events with 3 or 4 muon tracks in the pixel detector were collected.
In June 2008, during the beam injection tests, the SPD recorded in self-triggering mode the first events related to the beam activity in LHC. In September 2008, during the first circulating beams, the ALICE Inner Tracking System observed the first beam induced interactions: the trigger was provided by the PIT and based on a multiplicity algorithm.

Author: Ms CAVICCHIOLI, Costanza (CERN)

Presenter: Ms CAVICCHIOLI, Costanza (CERN)

Session Classification: POSTERS SESSION

Track Classification: Trigger