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SuperNemo Absolute Time Stamper, a high resolution and large dynamic range TDC for SuperNemo experiment

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The SNATS chip is designed to provide both a high resolution of 70ps RMS and a large dynamic range of 53 bits.

The architecture is based on the association of 32 cell delay locked loops and of a 48-bit digital counter which are synchronized to a 160 MHz external clock.

A 16 channel prototype has been designed in AMS 0.35 µm CMOS technology and its main performances are a Differential Non Linearity of about 0.2 LSB and an Integral Non Linearity about 1.3 LSB.

The circuit uses 12.7 mm2 of silicon area and is packaged in a 100-pin ceramic CQFP.

Summary

The aim of the NEMO collaboration is to investigate neutrinoless double-beta decay. This research is one of the principal topics in neutrino physics, which is a subfield of particle physics with cosmological and astrophysical implications.
Double-beta decay experiments can play a particularly interesting role in providing the answers to questions on the nature of the neutrino. Of paramount importance is the identification of the neutrino as a Dirac particle or Majorana particle.
For double-beta run of the SuperNEMO experiment, it has been decided to work without trigger module, with absolute time measurements.
To assume this requirement, a time stamp system is needed for the calorimeter front-end electronics.

So, the SNATS chip, described in this paper, has been designing to provide both a high resolution of 70ps RMS and a large dynamic range of 53 bits.
The architecture is based on the association of delay locked loop and digital counter which are synchronized by a 160 MHz external clock.
A prototype chip of 16 channels TDC was designed in AMS 0.35 µm CMOS technology.

The chip contains 8 DLL 's single ended (1 DLL for 2 channels) and a common counter. Each Delay Locked Loop has 32 delay elements giving a binning of 200 ps. To guarantee this binning independent of process and temperature variation, specific voltage controlled delay cell has been optimized. This cell is made of a current-starved inverter followed by a standard inverter.
Separate buffering of the outputs driving the channel buffers and the phase detector are required to maintain correct path delay matching and to minimize the effects of parasitic components.
The characteristic of the delay cells offers a low slope of 0.15ps/mV at typical frequency of 160 MHz which minimizes the jitter at the end of the DLL.
The memorization of the state of DLL's is obtained by 2 cascaded D latch in order to reduce metastability.
Voltage controlled external tuning is optionally available to reduce individually the phase error of each DLL and to optimize the Differential Non Linearity.
A 48 bits GRAY counter filling a 780um x 100um area, is employed for coarse conversion and used to measure a time range of about 20 days. It permits limiting the digital noise by decreasing the power consumption of the counter and its respective output buffers. The counter is composed of 12 parts modulo 4 bits to reduce the complexity and to insure the gear until a frequency of 200MHz.
In order to avoid error junction due to the phase difference between the DLL and the counter, a synchronizer was implemented to reduce the area used by limiting the use of two counters synchronous to opposite phases of the reference clock. The principle of this synchroniser consists in generating a hit coarse delayed in function of the relative position of the hit arrival within the clock period. It always permits latching the state of the counter when its outputs are in relation with the DLL.

When a channel is hiting, data are available with 4 words of 16 bits and 100ns are necessary to read its. After the read out, each channel must be reset to accept new event.

`Concerning the performances, it has been measuring a Differential Non Linearity of about 0.2 LSB and an Integra`

The static power dissipation is measured as about 380mW. The circuit uses 12.7 mm2 of silicon area and was packaged in a 100-pin ceramic CQFP.

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