Contribution ID: **104** Type: **Oral**

HARDROC, Readout chip of the Digital Hadronic Calorimeter of ILC

Tuesday 22 September 2009 15:50 (25 minutes)

HARDROC (HAdronic Rpc Detector ReadOut Chip) is the very front end chip designed for the readout of the RPC or Micromegas foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider.
The very fine granularity of the ILC hadronic calorimeters (1cm2 pads) implies a huge number of electronics channels (400 000 /m3) which is a new feature of "imaging"calorimetry.
Moreover, for compactness, the chips must be embedded inside the detector making crucial the reduction of the power consumption to 10 µWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).
HARDROC readout is a semi-digital readout with two or three thresholds (2 or 3 bits readout respectively in hardroc1 and hardroc2) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.
The 64 channels of the 2nd prototype, HARDROC2, are made of:
• Fast low impedance preamplifier with a variable gain over 8 bits per channel
• A variable slow shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 15pC.
• 3 variable gain fast shapers followed by 3 low offset discriminators to autotrig down to 10 fC up to 10pC. The thresholds are loaded by 3 internal 10 bit- DACs and the 3 discri outputs are sent to a 3 inputs to 2 outputs encoder
• A 128 deep digital memory to store the 2*64 encoded outputs of the 3 discriminators and bunch crossing identification coded over 24 bits counter.
• Power pulsing and integration of a POD (Power On Digital) module for the 5MHz and 40 Mhz clocks management during the readout, to reach 10µW/channel
The overall performance of HARDROC will be described with detailed measurements of all the characteristics. Hundreds of chips have indeed been produced and tested before being mounted on printed boards developed for the readout of large scale (1m2) RPC and Micromegas prototypes. These prototypes have been tested with cosmics and also in testbeam at CERN in 2008 and 2009 to evaluate the performance of different kinds of GRPCs and to validate the semi-digital electronics readout system in beam conditions.

Author: Mrs SEGUIN-MOREAU, Nathalie (OMEGA/LAL ORSAY/IN2P3)

Co-authors: Dr DE LA TAILLE, Christophe (OMEGA/LAL ORSAY/IN2P3); Mr DULUCQ, Frédéric (OMEGA/LAL ORSAY/IN2P3); Mrs MARTIN-CHASSARD, Gisèle (OMEGA/LAL ORSAY/IN2P3); Mr MATHEZ, Hervé (IPNL LYON/IN2P3); Dr LAKTINEH, Imad (IPNL LYON/IN2P3); Dr BRIENT, Jean-Claude (LLR PALAISEAU/IN2P3); Dr BOUDRY, Vincent (LLR PALAISEAU/IN2P3)

Presenter: Mrs SEGUIN-MOREAU, Nathalie (OMEGA/LAL ORSAY/IN2P3)

Session Classification: Parallel session A2 - ASICs

Track Classification: ASIC's