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Wafer Screening of ABCN-25 readout ASIC

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The ABCN-25 chip was fabricated in 2008 in the IBM 0.25 micron CMOS process. One wafer was immediately diced to make chips available for evaluation with test PCBs and hybrids, programmes which are reported separately. Early indications based on the diced wafer suggested a percentage yield in the high nineties, however the community decided to screen the remaining wafers such that faulty die could be excluded from the module construction programme.

This paper documents the test hardware and software, the procedures used to perform the screening and gives a brief overview of results.

Summary

The ABCN-25 chip was fabricated in 2008 in the IBM 0.25 micron CMOS process. One wafer was immediately diced to make chips available for evaluation with test PCBs and hybrids, programmes which are reported separately. Early indications based on the diced wafer suggested a percentage yield in the high nineties, however the community decided to screen the remaining wafers such that faulty die could be excluded from the module construction programme.

The objective of the screening is to identify ASICs for which all features needed for operation on a hybrid are functional. In addition to detailed (but not parametric) testing of the digital functionality, DAC characterisation and verification of the Serial Powering functions of the chip, basic analogue tests will also be made.

The wafers will be screened using a Cascade S300 automatic probe station at the STFC Rutherford Appleton Laboratory. This system has a 12" chuck, so may easily accommodate the 8" ABCN-25 wafers. A custom probe card has been produced to our specifications by Rucker and Kolls. This card does not use an edge connector, instead 0.1" headers are used to connect directly to ribbon cables. This allowed the probe card to be shortened, whilst giving improved vertical clearance over the wafer surface.

The readout hardware utilises commercial units. Fast LVDS signals are generated and received by a National Instruments 6562 PCI card, with 16 LVDS channels running at up to 200MHz. Slow TTL signals are generated by a National Instruments 6509 PCI card. An Agilent 34401A DVM is used to measure the DAC characteristics of the ABCN-25 chip, and a Thurlby Thandar TSX3510P programmable power supply is used to power the chip and to perform basic tests of its serial powering features.

A custom driver board was made by the University of Cambridge to link the hardware together. Based around a Xilinx Spartan 3 series FGPA, it performs the necessary signal buffering and level translation, connecting to the probe card (or a single chip test PCB) using short lengths of twisted pair cable. The FPGA firmware also enables some of the "slow" control signals to be driven under control of the "fast" interface, a useful means to improve the speed of certain digital test vector blocks, for example those involving changes of the chip's address lines. The card has also been designed such that all single ended CMOS control lines which go to the chip may be driven at 2.5V to suit ABCN-25 or at a lower voltage to suit future generations of the ATLAS strip readout ASIC.

The software used for wafer screening is a development of the SCTDAQ software used during the hybrid and module production phase of the present SCT detector. It has been extended for use with ABCN-25 and, optionally, to use the hardware outlined above in place of the custom VME modules used previously. ROOT is used to handle graphics, analysis, and the persistent storage of data.

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