# A digital calorimetric trigger for the COMPASS experiment at CERN

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## Overview

- The COMPASS experiment at CERN
- Motivation
- The electromagnetic calorimeter of COMPASS
- Digital contra analog trigger
- Trigger concept
- Trigger implementation
- Monitoring of the calorimetric trigger
- Conclusion/Outline

# The COMPASS experiment at CERN

#### Overview

- Common Muon and Proton Apparatus for Structure and Spectroscopy
- Fixed target experiment
- Super Proton Synchrotron at CERN

Physics program

- Spin structure of the nucleon
   → muon beam: up to 5.10<sup>7</sup>/s
- Hadron spectroscopy
  - $\rightarrow$  hadron beam: up to 5.10<sup>6</sup>/s

SPS

# The COMPASS Experiment at CERN

Setup:

- Two-stage magnetic



# Motivation

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Reactions producing a hard photon



Primakoff

DVCS

Deeply virtual Compton scattering

 $\Rightarrow$  Trigger on electromagnetic calorimeter (ECAL)

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# ECAL2

- Size: 2.44m×1.83m
- 3068 Cells (*64×48 2×2*):
  - 860 Shashlik modules -
  - 2208 GAMS modules
- 3072 Channels read out by Mezzanine Sampling ADC (MSADC)





# **12 bit SADC architecture**

RJ45/HL **Mezzanine SADC** USB 16/32 channels 12 bit 80/40 MHz Virtex4 CC4MSADC Virtex4 USB HotLink **TCS** receiver Power supplies **4 MSADC cards** 64 channels 12 bit

80 MHz

# Mezzanine sampling ADC





### Comparison of digital and analog trigger implementation

- Advantages of a digital trigger
  - More complex trigger logic achievable
    - Improved noise suppression
    - Amplitude normalization
    - Geometry (multi geometry settings possible)
  - Flexible settings (programmable)
    - Timing of channels
    - Thresholds
    - Calibrations
  - Better access in offline analysis
    - Monte Carlo
    - Trigger decision
  - High integration
    - Integrated into the readout system

# **Trigger concept**

- Energy summation over all included calorimeter channels
  - 2009: 16×16 central channels
  - Future: Extend to all 3068 channels of the calorimeter
- Trigger on events using a threshold on the total energy sum
  - Currently aimed at 20-40GeV (190GeV beam energy)
- On channel level:
  - Signal detection/zero suppression (constant fraction algorithm)
  - Time calculation and latency adjustment
  - Energy calibration

# Implementation:

- Pipeline algorithm for FPGA (on MSADCs)
- Parallel to readout logic on same FPGAs

#### Hardware overview

- Mezzanine Card:
  - Channel level:
    - Signal detection/zero suppression
    - Time extraction
    - Energy conversion
  - Sum over 16 Channels



# **Channel level computation**

- Pedestal subtraction
  - Pedestals updated upon each spill

# Constant fraction discriminator plus threshold

- Signal detection/zero suppression
- Time calculation
- Amplitude extraction
- Configurable

# Signal Time extraction

- Constant fraction discriminator
   B[i] = kA[i] A[i+N]
- Coarse Time : B[i] > 0 & B[i+1]≤ 0
- Fine Time : dt = B[i]/(B[i] - B[i+1])
- Trigger if A[i+M] is over threshold
- A[i+M] taken as signal amplitude (if triggered)



# **Channel level computation**

# Pedestal subtraction

- Pedestal updated upon each spill

# Constant fraction discriminator plus threshold

- Signal detection/zero suppression
- Time calculation
- Amplitude extraction
- Configurable

# Energy calibration

- Using energy calibrations for each individual channel
- Continuously monitored (online data processing)

# • Correct time dispersion of channels

- Using time calibrations on channel base
- Continuously monitored (online data processing)



## Implementation on Mezzanine card



+ Sum 16

### Hardware overview

- Mezzanine Card:
  - Channel level:
    - Signal detection/zero suppression
    - Time extraction
    - Energy conversion
  - Sum over 16 Channels
- VME module:
  - Sum over 64 Channels
  - Output to backplane



### Hardware overview

- Mezzanine Card:
  - Channel level:
    - Signal detection/zero suppression
    - Time extraction
    - Energy conversion
  - Sum over 16 Channels
- VME module:
  - Sum over 64 Channels
  - Output to backplane
- Backplane summation cards
  - Final summation
  - Apply threshold (output NIM)
  - Extendable by interconnection



# System architecture in 2009



# Monitoring

# • Monitor and generate calibration constants continuously

- Using online data processing (PC farm)
- Monitor LED pulses to adjust energy calibrations
- Extract timing of channels
- Updated once per run (about 2h)
- Stored values in VME registers
  - Independent communication
  - Scaler (channel)
  - Current pedestals
  - Readout once per spill
- Hit Time and Amplitude added to corresponding event into data stream for online/offline analysis

# **Conclusion/Outlook**

- Digital trigger logic on FPGA
  - Implemented on electronics developed for ECAL readout (12bit, 80MHz SADC)
  - Pipelined CFD based algorithm
  - Time resolution better than *1ns*
  - Architecture scalable
  - Expected trigger rates for COMPASS ca. 25kHz@30GeV threshold (190GeV/c hadron beam)
- Schedule
  - Start of project mid December 2008
  - Test beam end of August 2009 (Analysis of data is currently ongoing)
  - First use in COMPASS foreseen for mid October 2009
- Upgrade options for future improvements
  - Include complete calorimeter (multiple summation ranges)
  - Clustering (improved noise suppression and energy calculation)

## Thank you for your attention!

# **Expected Trigger-Rates for ECAL2 (no coincidence)**

- Conditions:
  - Beam:
    - Intensity: **≈5**.10<sup>6</sup>/s
    - Particles:  $\pi$
    - Momentum: 190GeV/c
  - Target:
    - Cu 3.5 mm
    - ≈24% X<sub>0</sub>
    - ≈2.3% λ<sub>1</sub>
- Rates from simulation:

Threshold	FULL (64x48)	<b>16x16</b>
20 GeV	85.1 kHz	40.7 kHz
25 GeV	60.5 kHz	32.0 kHz
30 GeV	36.7 kHz	25.6 kHz
35 GeV	28.6 kHz	21.0 kHz
40 GeV	22.9 kHz	17.3 kHz
60 GeV	10.2 kHz	8.4 kHz
80 GeV	5.0 kHz	4.3 kHz



# Energy comparison between online (FPGA) and 'offline' (float)



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150 ns

# Time constrains for trigger (estimation)

- Time of flight (Target to ECAL2): 115 ns
  Signal generation (Detection to ADC): 120 ns
  ADC digitalization: 200 ns
- Run time trigger signal to trigger barrack: 200 ns
- Trigger decision in FPGA clock cycles (@80MHz)
  - Channel computation: 1-3 (depends on implementation, might be combined with digitalization)
  - Delay to synchronize signals: 1-3 (foreseen, synchronizes most channels)
  - Mezzanine (Sum over 16 channels): 3 (might even be combined with earlier)
  - VME module (Sum over 64channels): 2
  - Sum over all channels: <=1</li>

#### ⇒ ≈ 12·12.5 ns =

- ⇒ Needed are **765 ns** to make decision. Currently there are about 500 ns to take a trigger decision. Increase to **1**  $\mu$ **s** to be on the save side.
- $\Rightarrow$  Digital trigger achievable with current ECAL2 electronics!!!









Total Energy [GeV]

Energy Sum (float) [GeV]