System Integration Issues of DC to DC converters in the sLHC Trackers

B. Allongue[a], G. Blanchot[a], F. Faccio[a], C. Fuentes[a,b], S. Michelis[a,c], S. Orlandi[a]
[a] CERN, 1211 Geneva 23, Switzerland
[b] UTFSM, Valparaiso, Chile
[c] EPFL, Lausanne, Switzerland
georges.blanchot@cern.ch

TWEPP 2009, Paris

Outline

- DC/DC Converters for Trackers at sLHC.
- System integration issues to be considered.
- Radiated couplings and inductor.
- Conducted noise and layout.
- Susceptibility of the ABCn hybrids prototypes.
- Conclusions

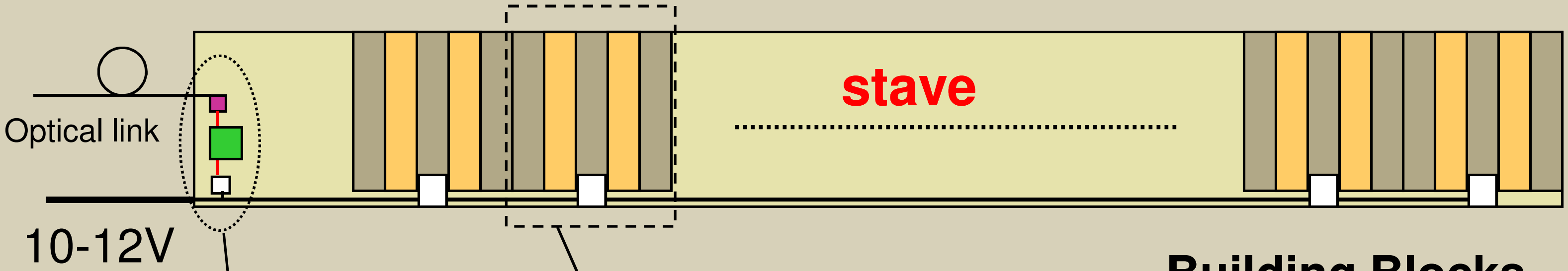
DC/DC Converters at sLHC

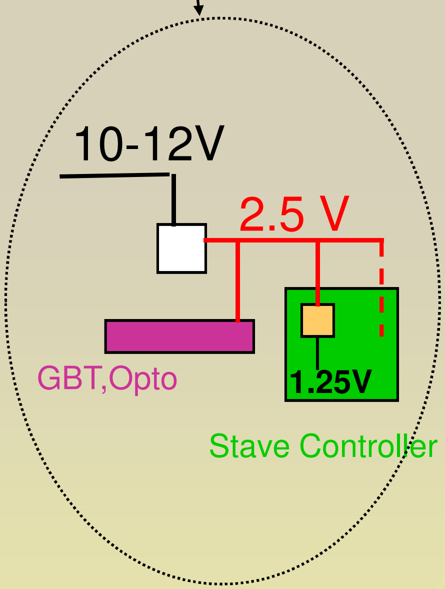
- **<u>Requirements:</u>**
  - To deliver increased amount of power.
  - To contain or even reduce thermal losses.
  - To minimize the material needed to bring the power in.
    - Cables
    - Boards
  - To be compatible with the environment
    - Radiation,
    - Magnetic field
    - Space
  - Not to inject noise in the system.
- A **powering scheme** based on DC/DC converters that fulfill these requirements is proposed.

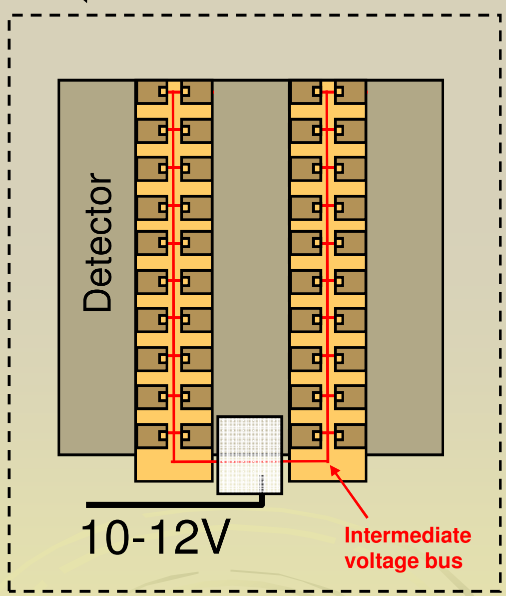
Powering Scheme at sLHC

Distribution based on 2 conversion stages

Example design shown for ATLAS short strip concept







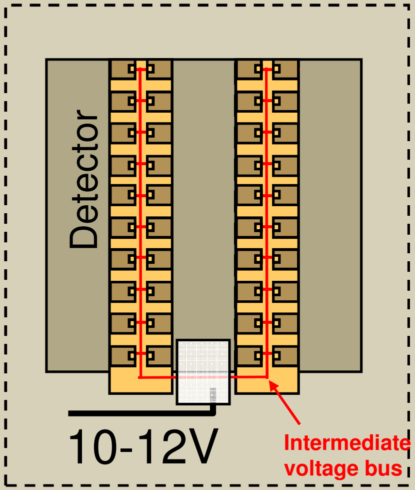
Building Blocks

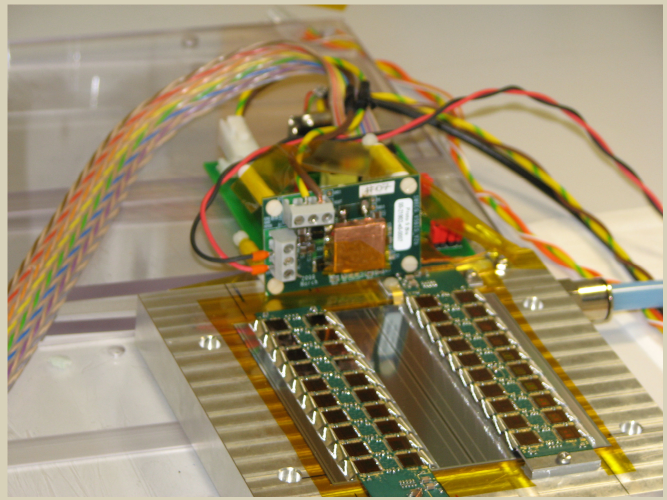
Stage1:
- Inductor-based buck
- Vin = 10-12 V
- Vout = 2.5-1.8 V
- Pout = 2-4 W

Stage2:
- On-chip switched capacitor
- Vin = 2.5-1.8 V
- Conversion ratio ½ or 2/3
- Iout = 20-100 mA

Same blocks can be combined differently to meet custom system requirements

System Integration Issues

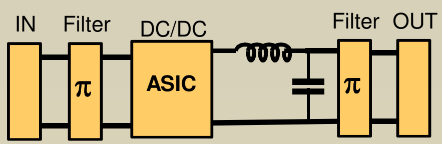


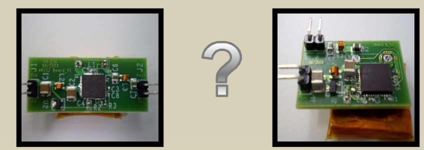


To which noise sources is the system sensitive and how much ?

What are the noise sources of the converter and how to quantify them ?

The proposed scheme requires to have the converter very close to the detector and ASICs.





What is the best layout ?

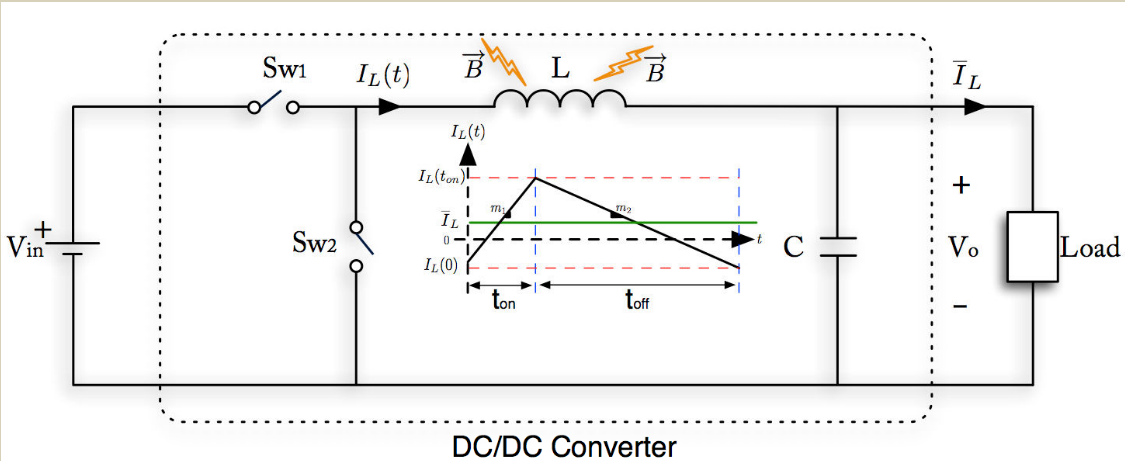
- The DC/DC noise must be minimized.
- The immunity of the system against couplings must be maximized.

What is the best inductor ?

Outline

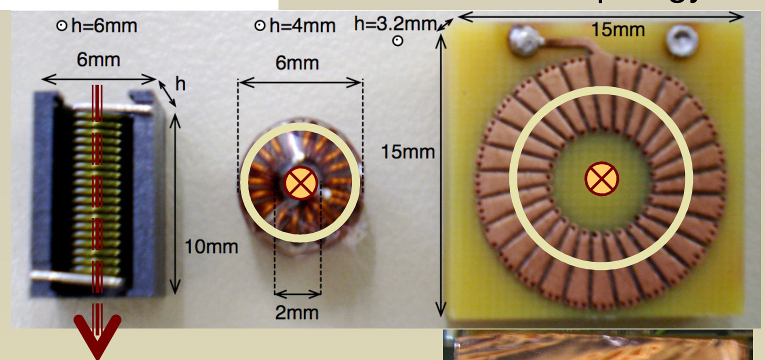
- DC/DC Converters for Trackers at sLHC.
- System integration issues to be considered.
- Radiated couplings and inductor.
- Conducted noise and layout.
- Susceptibility of the ABCn hybrids prototypes.
- Conclusions

Radiated Couplings and Inductor



A triangular current at switch frequency, whose amplitude is of few amperes, flows in the DC/DC output inductor.

This results in a radiated magnetic field, whose direction and intensity will strongly depend on the inductor topology.



Compared topologies:

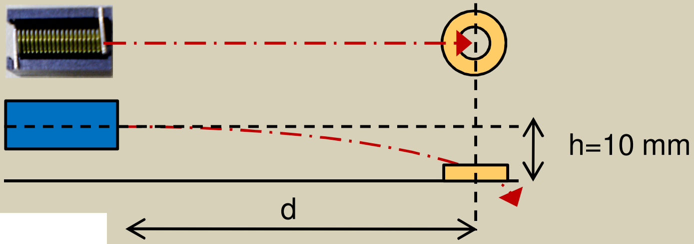
- Solenoid, 500 nH, the full magnetic field is radiated along its axis (N loops). Shielding not possible without reducing the inductance value.

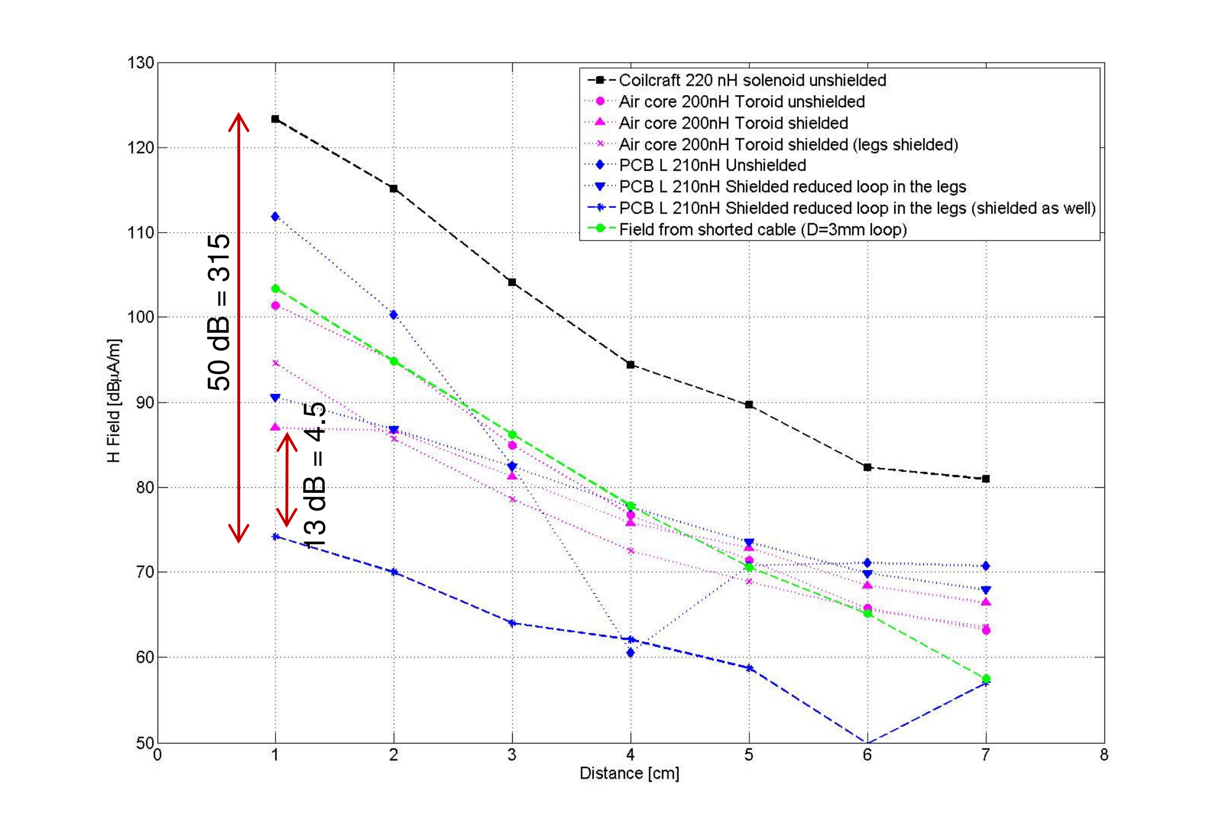
- Air core toroid, 200 nH, main field is confined in the toroid volume; residual field due to current along the tore axis (1 loop). Shielding possible.

- PCB toroid, 500 nH, geometry limited by PCB technology. Shielding possible in the PCB layers.

Radiated Couplings and Inductor

H Field measured with calibrated and amplified loop probe:
- solenoid, air core toroid, PCB toroid.
- shielding of coil, shielding of pins using 35 um copper foils.





- ➢ Solenoid is the most noise and can't be shielded.
- ➢ Air core toroid is good and shield reduces furthermore the field.
- ➢ PCB toroid is very effective if shielded. *It has more than 300 times less noise than the solenoid and 4 times less than the shielded air core toroid.*
- ➢ The loop formed by the inductor pins is a non negligible source of H field: the connection pins must be shielded too.

Outline

- DC/DC Converters for Trackers at sLHC.
- System integration issues to be considered.
- Radiated couplings and inductor.
- Conducted noise and layout.
- Susceptibility of the ABCn hybrids prototypes.
- Conclusions

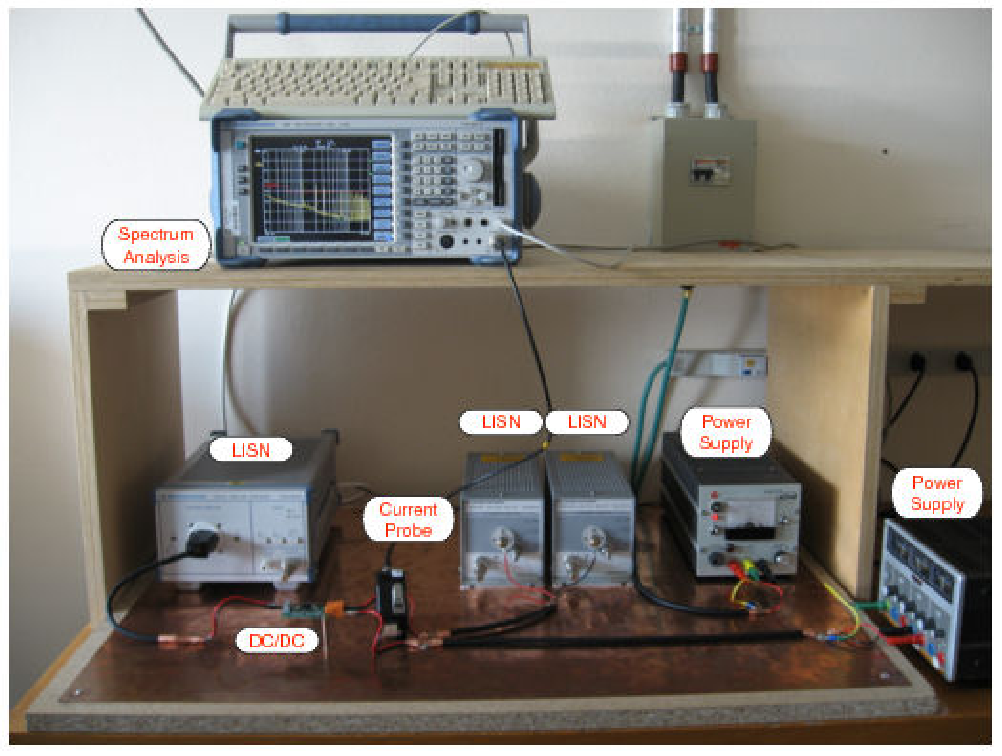
Conducted Noise

Conducted noise is emitted in the form of currents by the converter into the cables:

- Differential Mode Noise (ripple)
- Common Mode Noise (in GND plane).

It is measured on a dedicated setup, that uses Line Impedance Stabilization Networks to normalize the measurement.

The measurement is made with calibrated current probes and on the LISN ports.

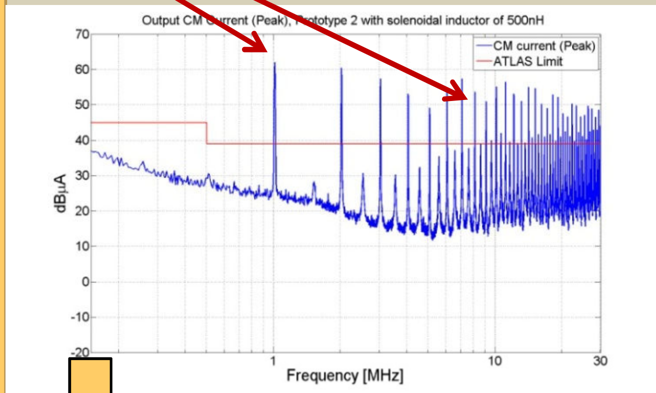


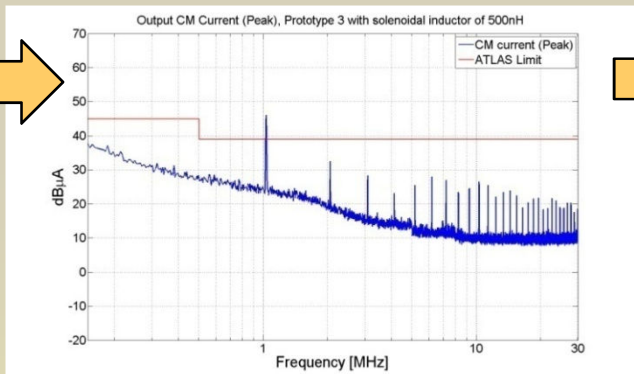
The conducted noise was radically reduced on past prototypes.
It was found that the layout and the placement of components is determinant to reduce the conducted noise.

Performance of DC/DC Prototypes

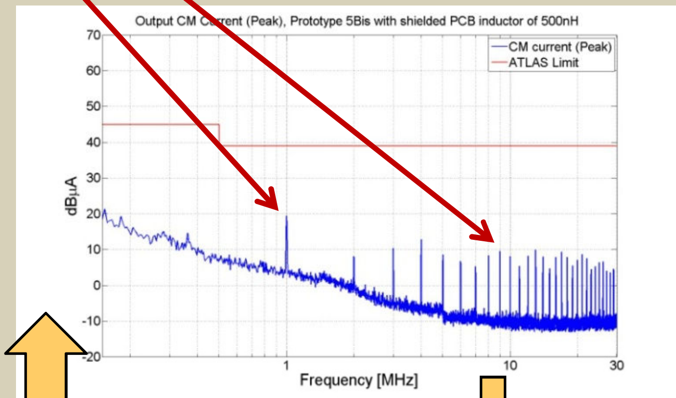
Proto#2 reached 60 dBuA = 1mA at Fsw

Proto#2 reached 50 dBuA = 320uA at 10 MHz

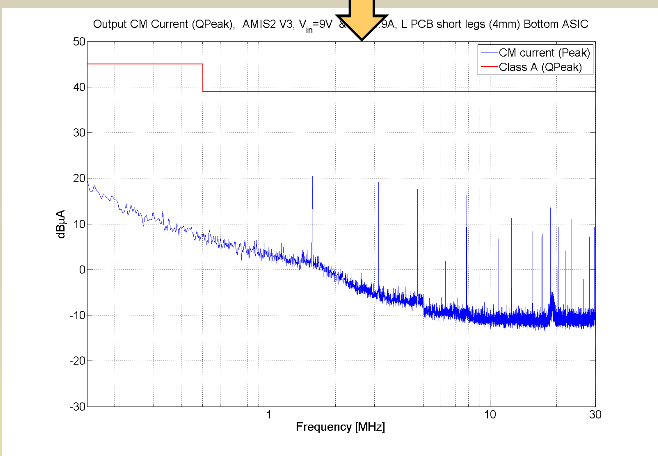




Proto#5 reaches 25 dBuA = 17uA at Fsw, and 10 dBuA = 3uA at 10 MHz: ***the emission of CM current has been reduced by an order of more than 50 at switch frequency, and by two orders of magnitude at 10 Mhz.***

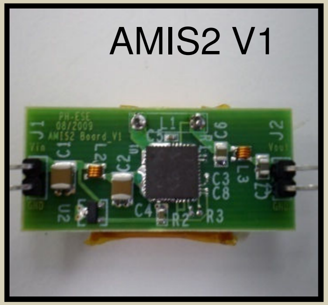


Significant noise reduction in Proto#3



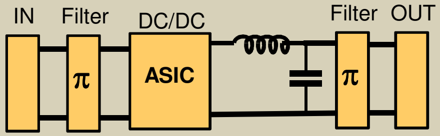
Low Noise was also achieved with the AMIS2 ASIC Prototype

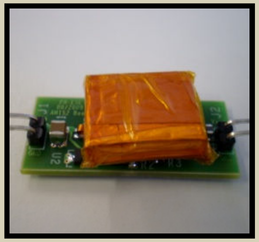
AMIS2 Tests: Layout

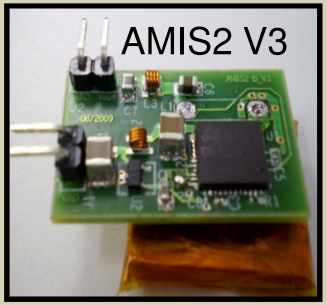


In/Out on opposite sides

Filters on opposite sides







In/Out on corner sides

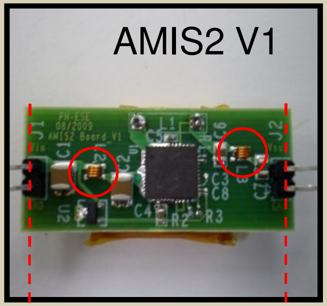
Filters close together

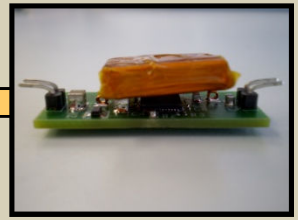
Several layouts have been tried for the same schematic using the AMIS2 ASIC. Comparison of two of those are shown here:

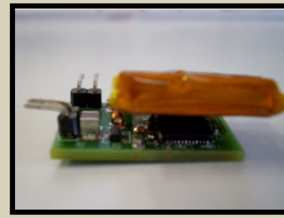
- Separated input and output (and filters).
- Input and Output close together.

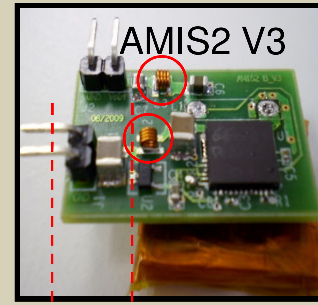
Different positions and types of the coils were tried.

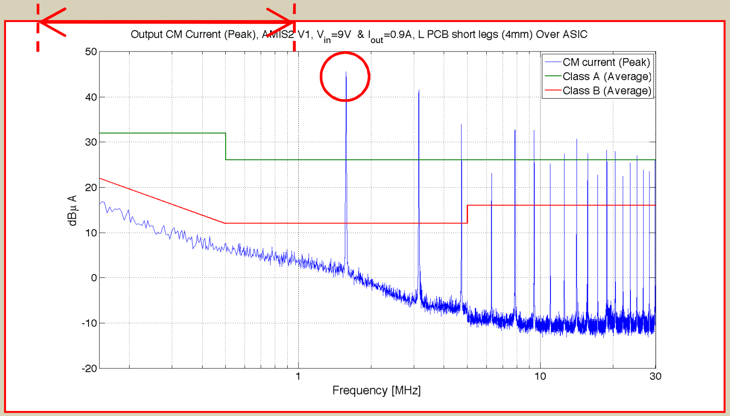
AMIS2 Tests: Layout Issues



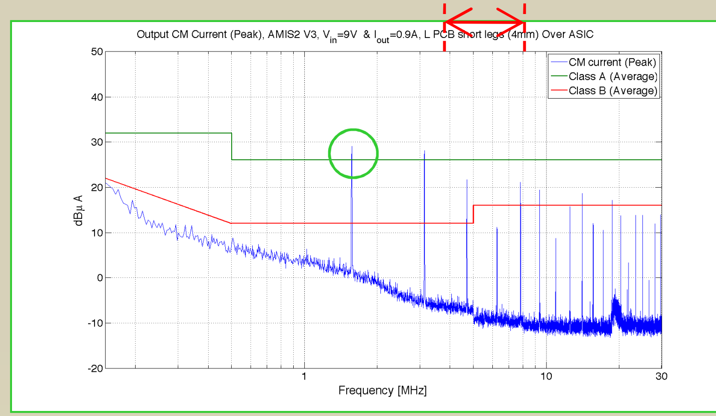


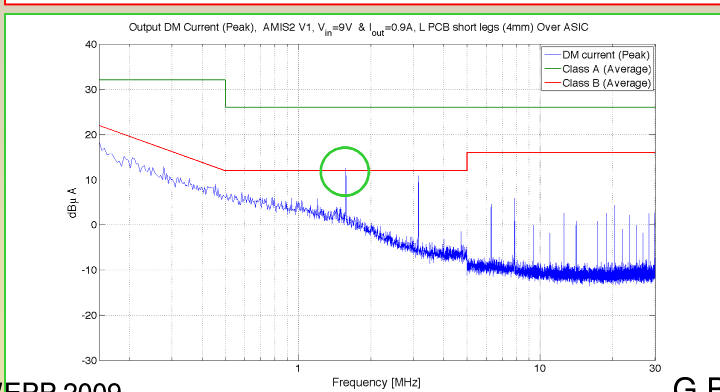




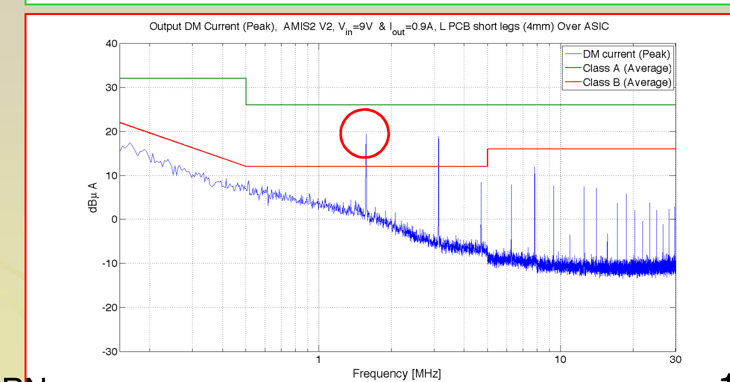


CM

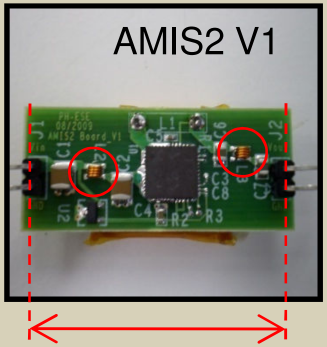


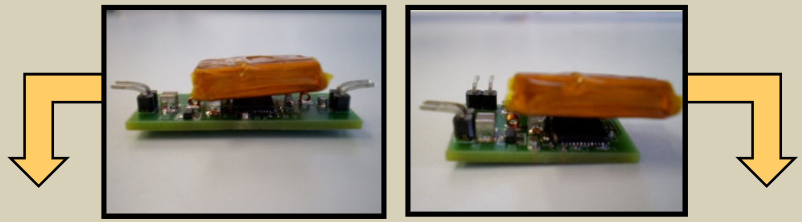


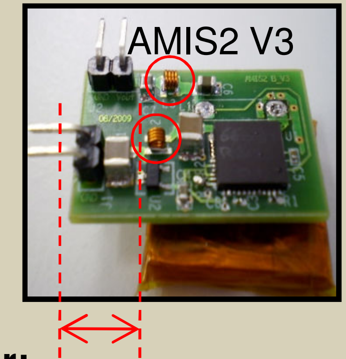
DM



AMIS2 Tests: Layout Issues







<u>In/Out Separation:</u>

- Large distance between In/Out GND pins:
  - *Vcm = Lgnd*(dI/dt) develops between the pins and leads to worse CM noise.*

- But the distance between In/Out filter reduces couplings between filter inductors:
  - *Good attenuation of ripple.*

- Easier to fit big coils on top side.

- *The performance could not be improved with different placements: the layout dominates noise performance.*

<u>In/Out Close Together:</u>

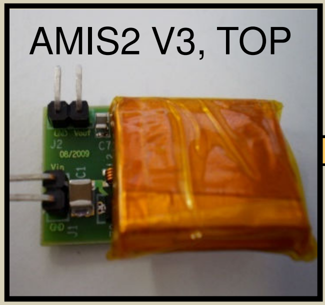
- Small distance between In/Out GND pins:
  - Lgnd is much smaller, therefore CM is reduced (10 dB to 15 dB).

- Proximity of In/Out filter and L inductors couples DM currents between In and Out.
  - Slightly worse DM attenuation.

- Difficult to fit big coils on top.
  - Stacked coils will couple.

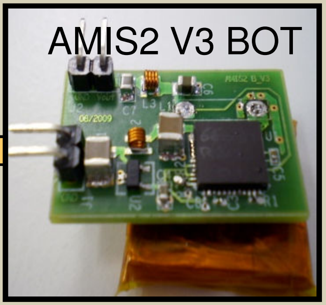
- *Room for improvements with different coil arrangements (see next).*

AMIS2 Tests: Coil Top/Bot

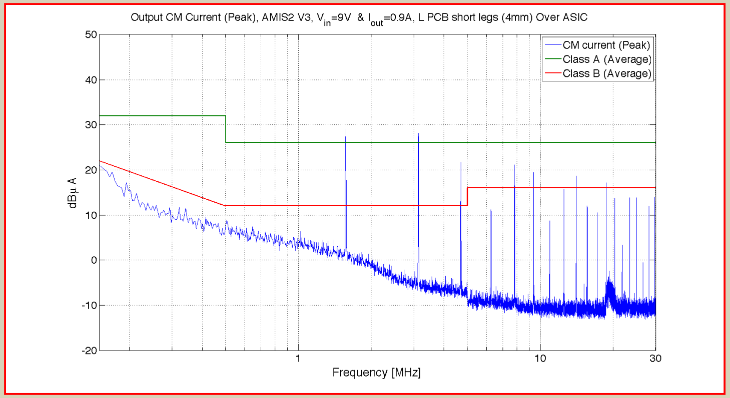


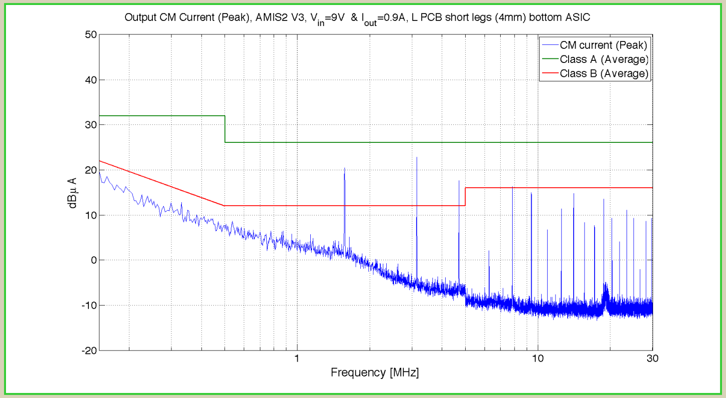
The placement of the coil has a negligible impact on V1 because the main inductor is at some distance of the pi filters, therefore there is not an important coupling.

This is not the case for V3, which has its noise dominated by couplings from the main coil.

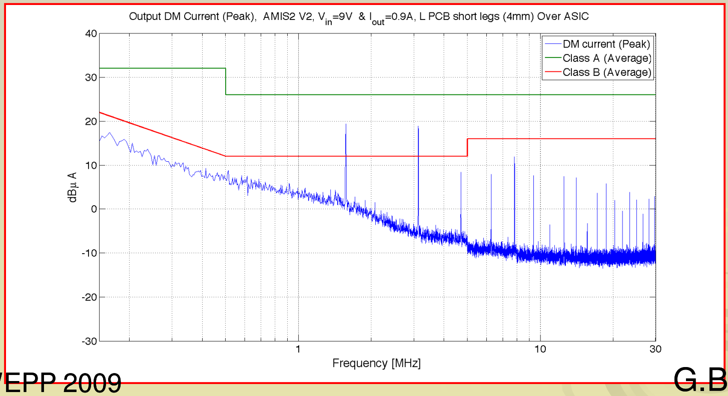


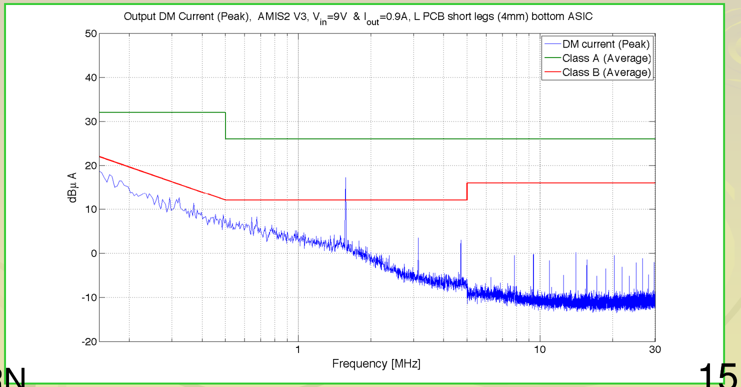
CM



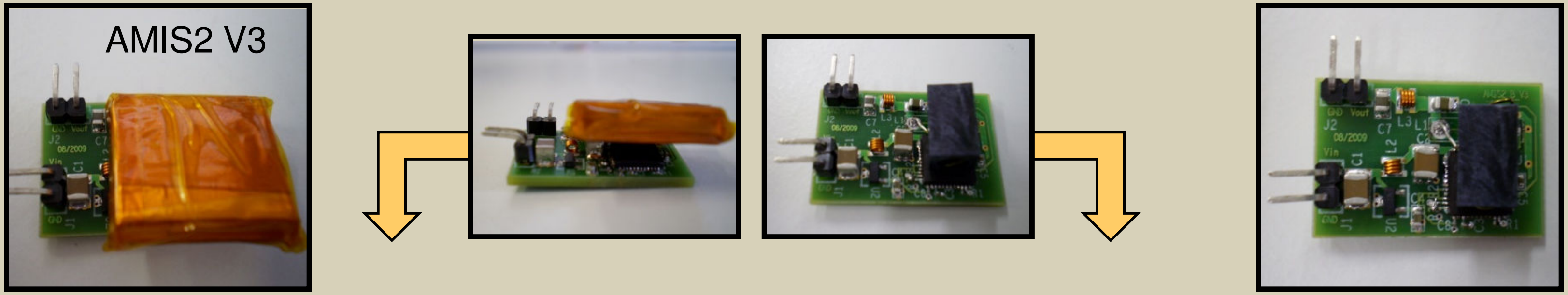


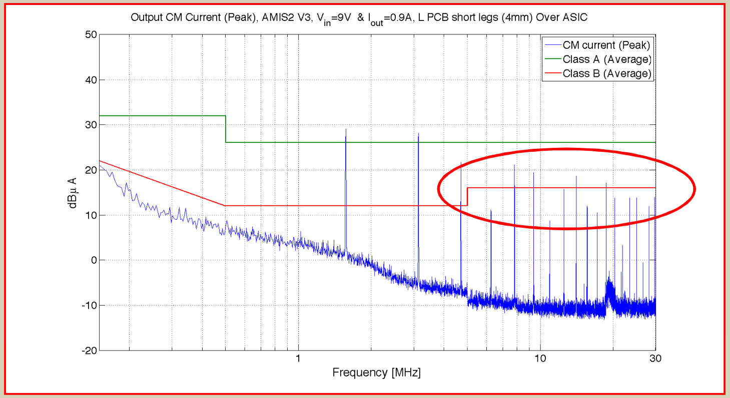
DM



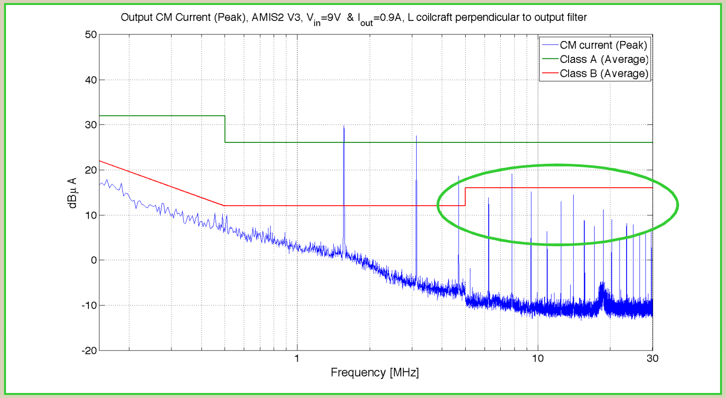


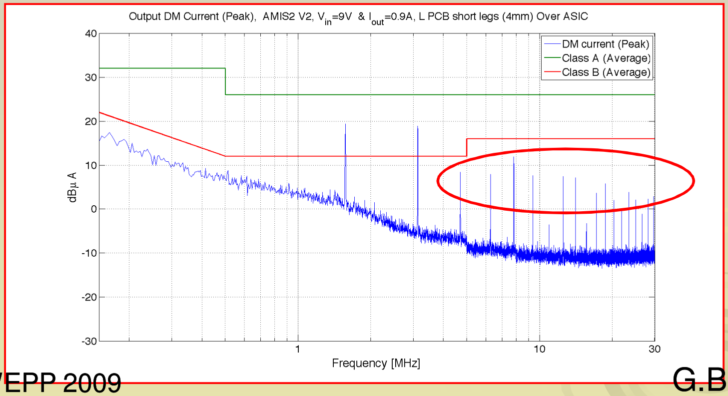
AMIS2 Tests: Inductor Type



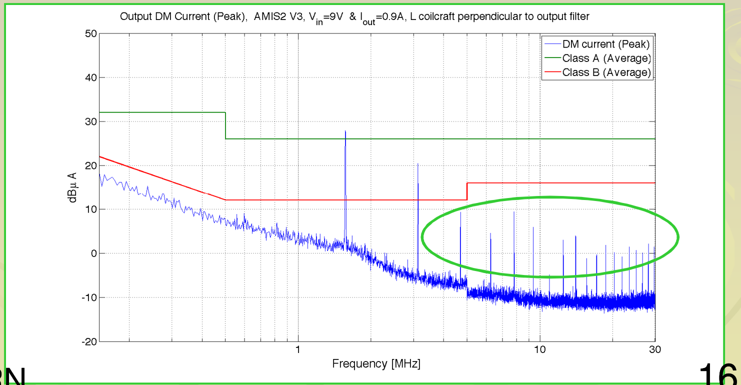


CM

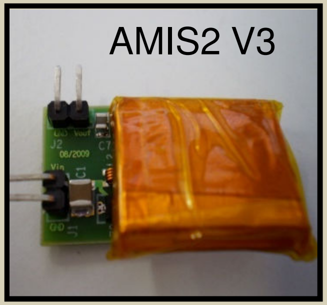


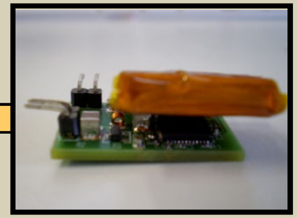


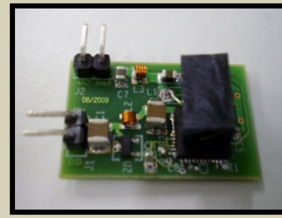
DM

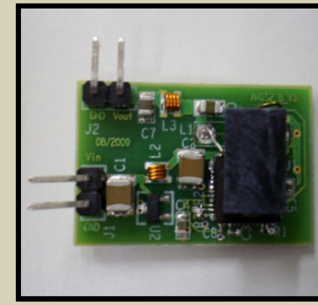


AMIS2 Tests: Inductor Type









PCB Inductor on top:

- CM performance of AMIS2 V3 is superior to V1 because of its layout.
- The PCB coil is very large for V3 board: it falls above the filter coils, which limits still the DM performance.
  - *Higher switching frequencies would allow reducing its size and reduce therefore the couplings*
- *It must be reminded that the shielded PCB coil radiates much less H field than its solenoid counterpart.*

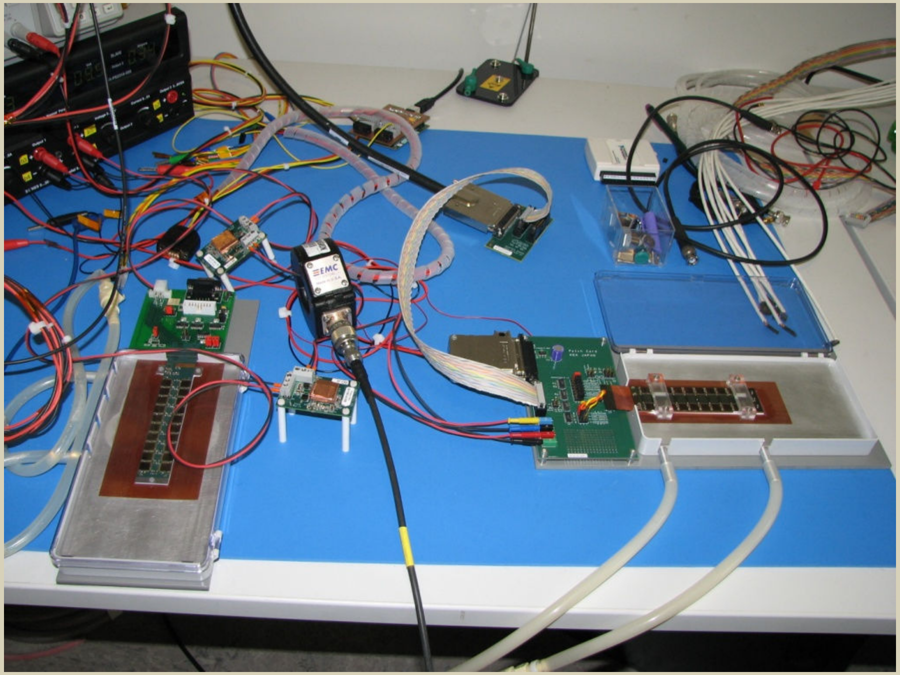
Solenoid Inductor on top:

- The CM looks very slightly better (few dB) at high frequencies.
- The coil is smaller and fits better above the ASIC: it is away of the filter coils which explains the better DM.
- The coil was oriented such that the main field stays away of the connectors and filters.
  - *But the main field is fully radiated towards the hybrid and detector.*

Outline

- DC/DC Converters for Trackers at sLHC.
- System integration issues to be considered.
- Radiated couplings and inductor.
- Conducted noise and layout.
- Susceptibility of the ABCn hybrids prototypes.
- Conclusions

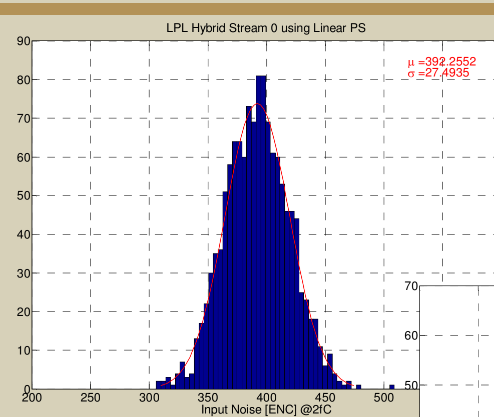
Tests with ABCn w/o strips



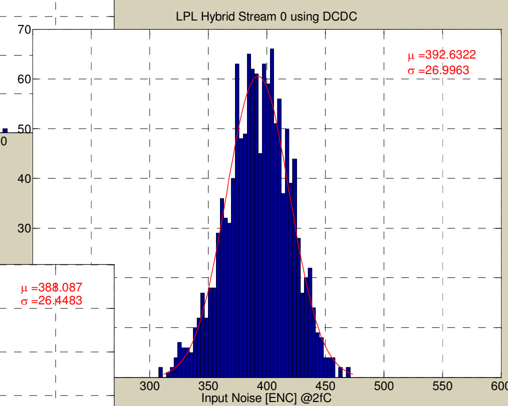
Two hybrid prototypes tested, 20 ABCn chips on each, 4A DC, without strips detector mounted:

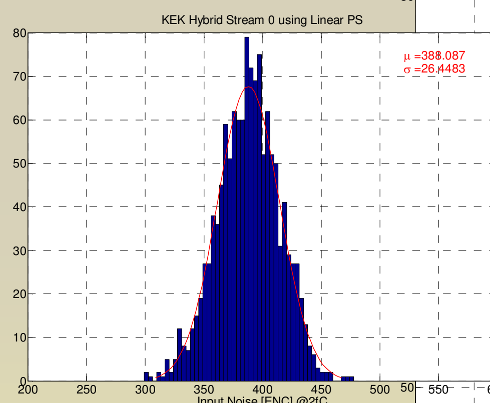
- Liverpool Hybrid, requires one DCDC or linear PS.
- KEK Hybrids, requires two DCDC or linear PS.
- Noise estimation: Qe*(RMS of fitted scurves)/Gain [ENC].

No noise degradation observed when using the DCDC, even when powering the analog part directly from DCDC (KEK case).

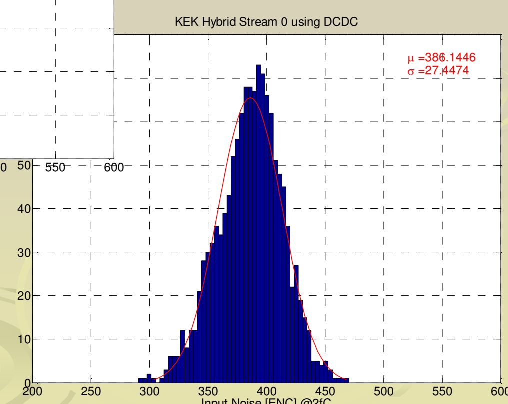


Liverpool Hybrid with linear PS and with DCDC

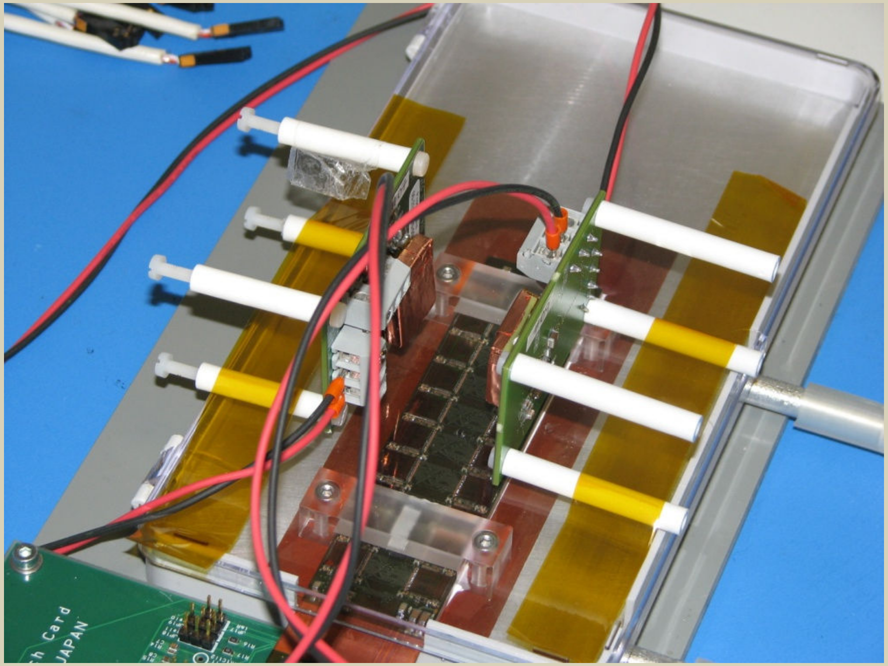




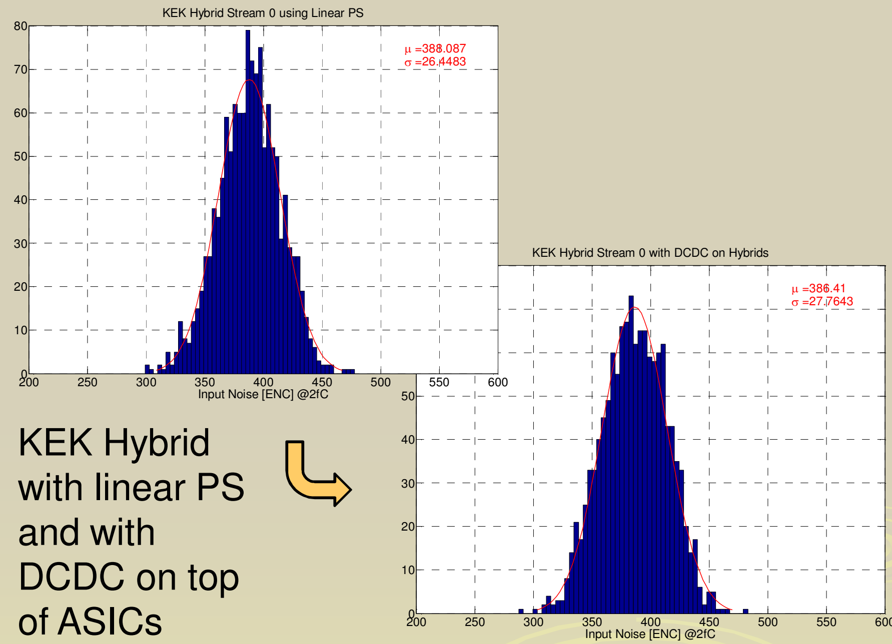
KEK Hybrid with linear PS and with DCDC



Tests with ABCn w/o strips (2)



Histograms are obtained from Scurve fits at 2 fC with non equalized gains.



Radiated coupling test on the KEK hybrid using two DCDC converters facing the ABCn chips.

KEK Hybrid with linear PS and with DCDC on top of ASICs

No observable noise degradation when exposed to DCDC magnetic field from coils.

Tests with ABCn w/o strips

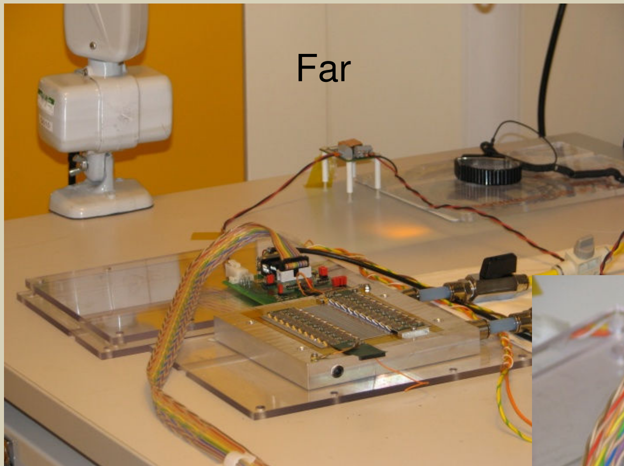
ENC at 2 fC	Average		RMS	
	Row 0	Row 1	Row 0	Row 1
LPL Linear PS	392.3	390.8	27.5	27.7
LPL DC/DC	392.6	390.9	27.0	27.9
KEK Linear PS	388.1	390.0	26.4	27.6
KEK DC/DC	386.1	387.0	27.4	26.0
KEK Edge	386.4	388.0	27.8	26.3

There has been no significant increment of noise neither due to conducted noise or to radiated couplings on the ASICs.

It must be noticed that the channels were not gain equalized: the gain dispersion can hide the noise sensitivity, if there is any.

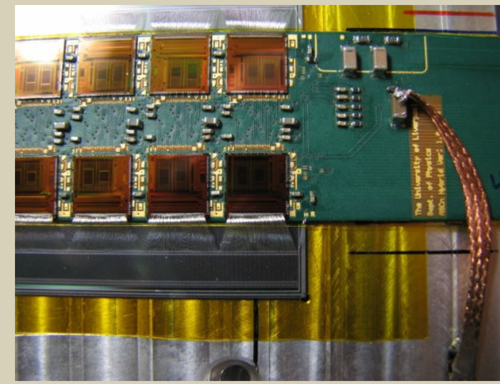
It must be noted also that the KEK hybrid powers the analog part of ABCn directly from a DCDC, while the Liverpool hybrid enables the ABCn LDO regulator.

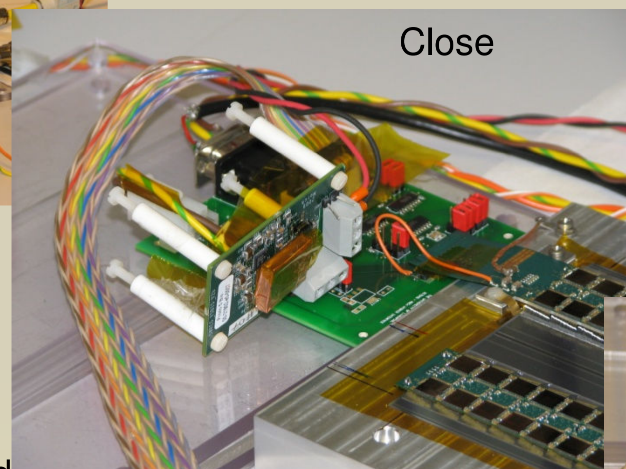
Tests with ABCn with strips



One out of two ABCn hybrids tested with the same DC/DC converters in three locations: far, close and on the strips edge.

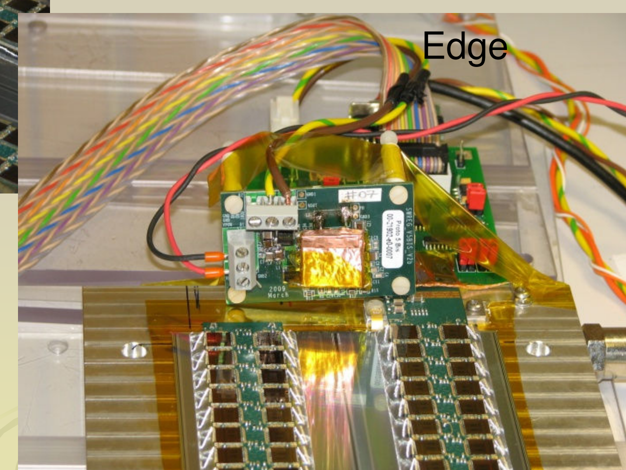
The hybrids are bonded to strips.





The gains are first equalized through a 3-point gains calibration run.

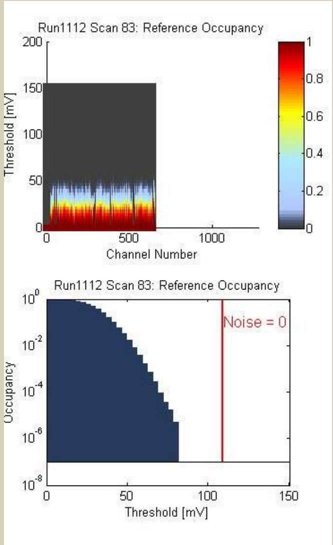
Afterwards, Scurves are obtained without charge to build up occupancy plots.



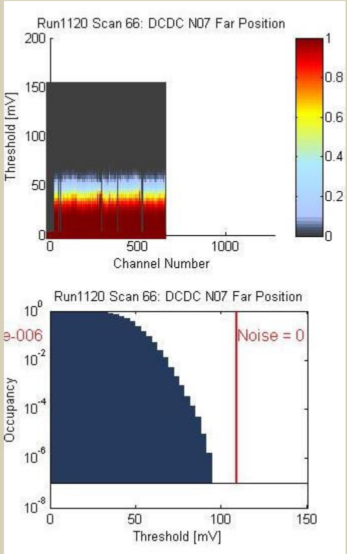
The noise is estimated as the occupancy for a threshold setting of about 110mV, which is equivalent to 1fC for equalized gains.

Tests with ABCn with strips

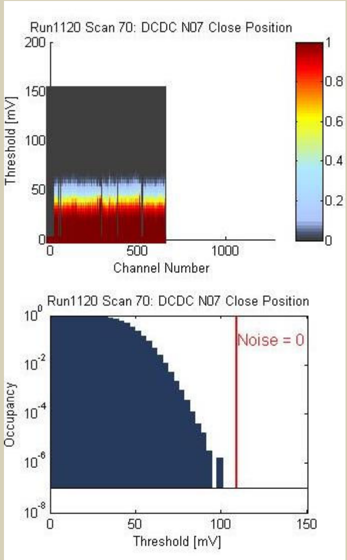
Reference



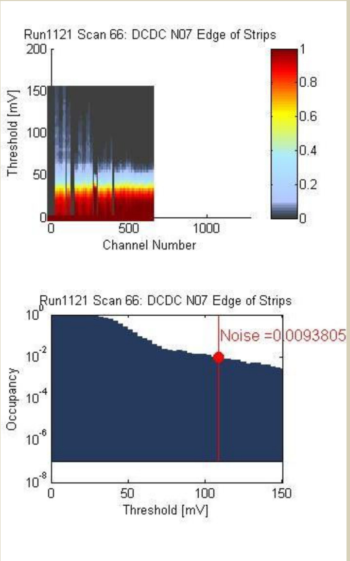
Far



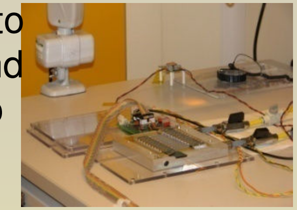
Close

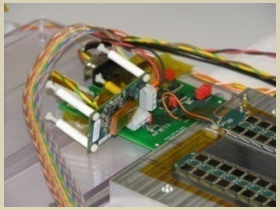


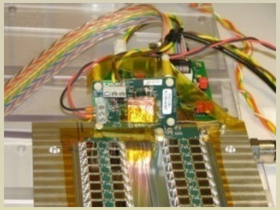
Edge



Linear PS: the Scurves fall to zero above Vth = 60 mV, and the occupancy noise is zero at 1fC equivalent.





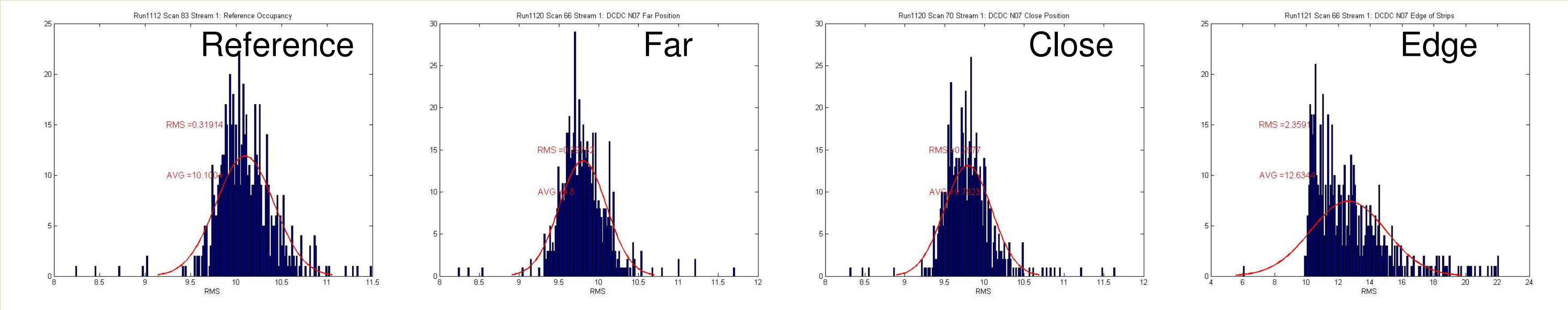


Occupancy charts are very sensitive to dead or unstable channels.

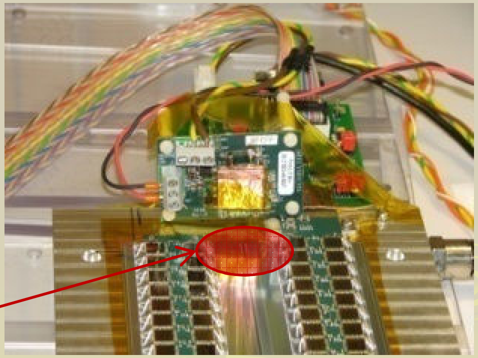
The occupancy expands to higher thresholds, but the effect becomes critical only if the coil is facing the strips.

Tests with ABCn with strips

Fitted S-Curves RMS distributions



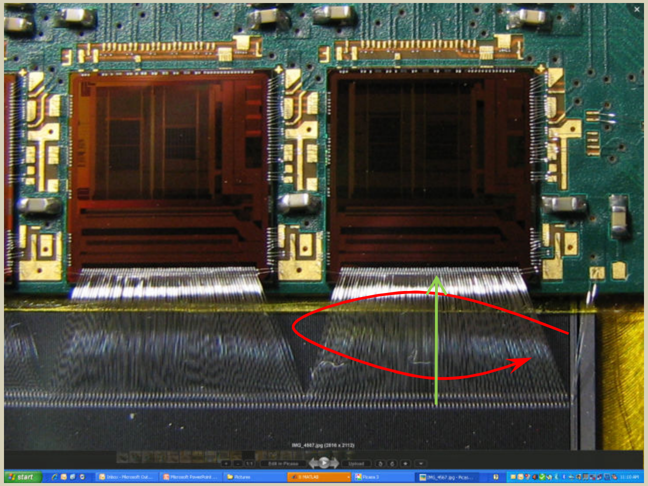
ENC*G/Qe	Average		RMS	
	Row 0	Row 1	Row 0	Row 1
Reference	10.2	10.1	0.41	0.32
Far	9.82	9.80	0.40	0.30
Close	9.80	9.79	0.38	0.30
Edge	10.1	12.6	0.37	2.36

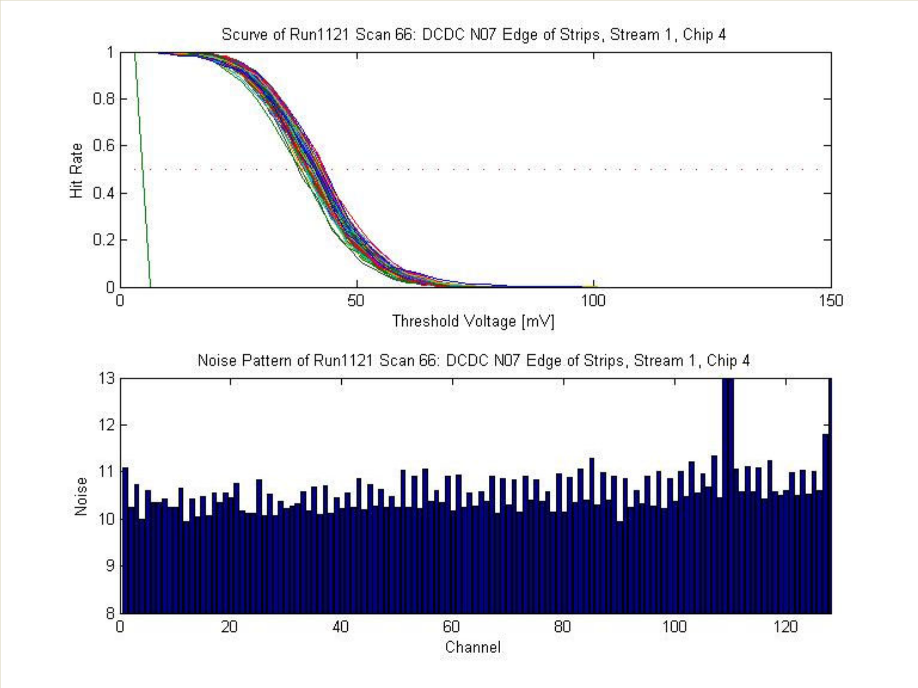


Sensitive area

Only the channels directly exposed to the inductor field (< 2cm, row 1) are sensitive to it.
The other channels are insensitive to it (row 1) even when the coil is facing the edge of the hybrid.

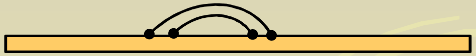
Impact of the bonding pattern





The bonding pattern is an alternating structure that forms a loop with the ground plane. The loop is exposed to B field from the converter and injects parasitic currents into the bondings.

The current is proportionnal to the loop area, resulting in a patterned noise structure.



Conclusions

- Different coil configurations were explored, looking for the minimum emitted magnetic field:
  - Solenoid discarded, Air core toroid is better.
  - Shielded PCB toroid brings the lowest emission, but hard to manufacture.
- Compact layouts help reducing the emission of noise:
  - Reduced ground inductance in power path = less CM noise.
  - In and Out must sit close together.
  - ASIC development favors reduction of noise emissions.
  - An increasing switching frequency would allow reducing L and C sizes.
- Noise susceptibility of tracking detectors is found at the signal input
  - Only sensitive if strips bonded.
  - Bonds are only sensitive to DCDC within a radius of 2 cm approx.
  - Shorter bonds, or alternative mounting options are the most efficient ways to improve the system immunity against noise.

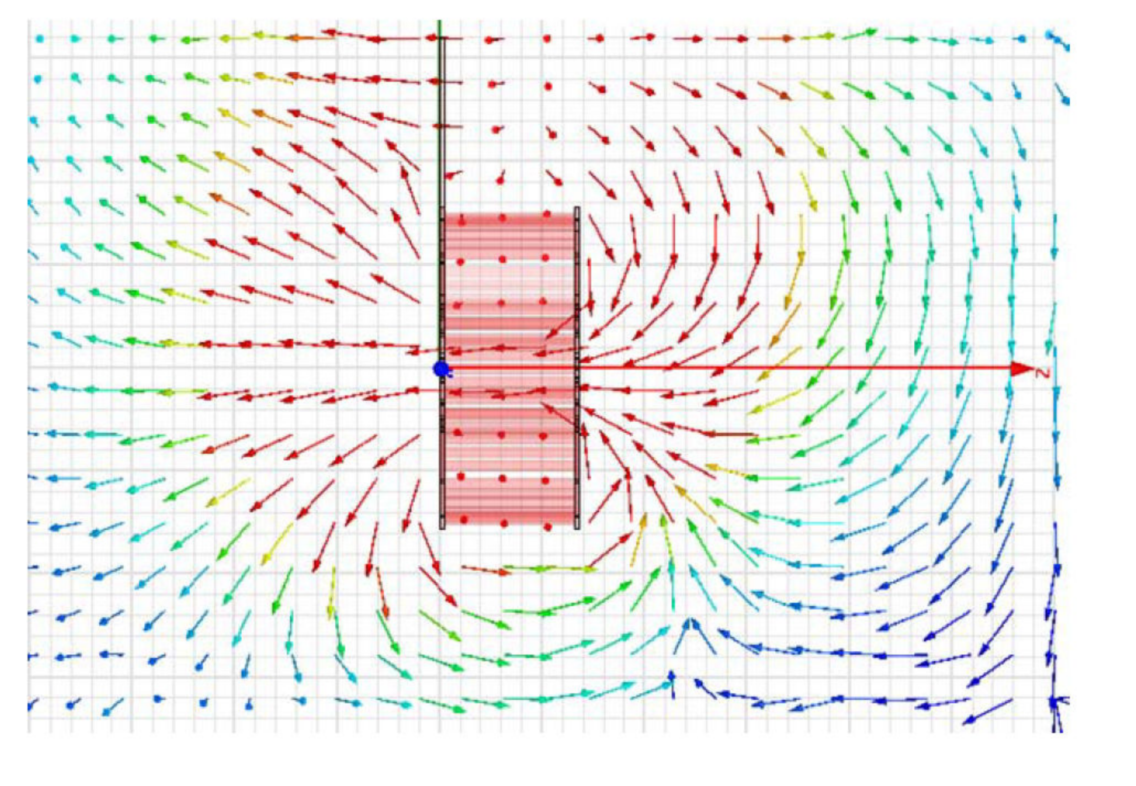
Backup Slide

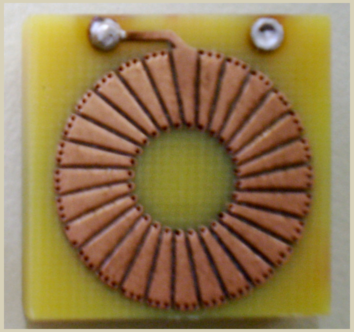
- Field Lines from Coils and symmetry issues

Optimization of shielded PCB air-core toroids for high efficiency dc-dc converters

S. Orlandi[1], B. Allongue[1], G. Blanchot[1], S. Buso[2], F. Faccio[1], C. Fuentes[1,3], M. Kayal[4], S. Michelis[1,4], G. Spiazzi[5]

[1] CERN
1211 Geneva 23
Switzerland
[2] Dept. of Technical Management of Industrial Systems - DTG University of Padova, Italy
[3] UTFSM, Valparaiso, Chile
[4] EPFL, Lausanne, Switzerland
[5] Dept. of Information





ECCE 2009 Conference, San Jose, CA, USA